

TOSHIBA CMOS DIGITAL INTEGRATED CIRCUIT SILICON MONOLITHIC

**TC74HCT540AP, TC74HCT540AF, TC74HCT540AFW**  
**TC74HCT541AP, TC74HCT541AF, TC74HCT541AFW**

**OCTAL BUS BUFFER WITH TTL INPUT LEVEL**  
**TC74HCT540AP/AF/AFW INVERTING, 3-STATE OUTPUTS**  
**TC74HCT541AP/AF/AFW NON-INVERTING, 3-STATE OUTPUTS**

(Note) The JEDEC SOP (FW) is not available in Japan.

The TC74HCT540A / TC74HCT541A are high speed CMOS OCTAL BUS BUFFERS fabricated with silicon gate C<sup>2</sup>MOS technology.

These devices may be used as a level converter for interfacing TTL or NMOS to High Speed CMOS. The inputs are compatible with TTL, NMOS and CMOS output voltage levels.

They achieve the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.

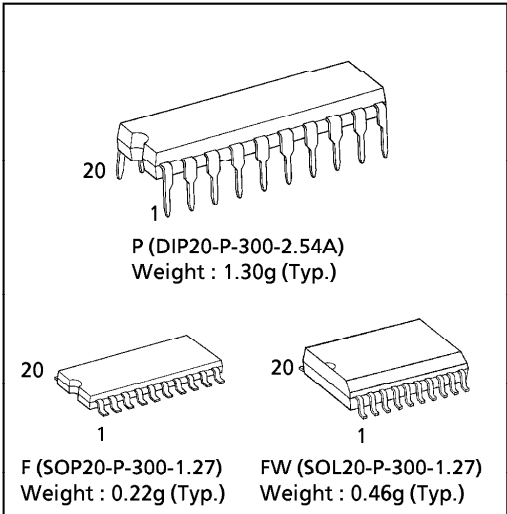
The TC74HCT540A is a non-inverting type, and the TC74HCT541A is an inverting type.

When either  $\bar{G}1$  or  $\bar{G}2$  are high, the terminal outputs are in the high-impedance state.

All inputs are equipped with protection circuits against static discharge or transient excess voltage.

**FEATURES :**

- High Speed.....  $t_{pd} = 10ns$  (typ.) at  $V_{CC} = 5V$
- Low Power Dissipation.....  $I_{CC} = 4\mu A$  (Max.) at  $T_a = 25^\circ C$
- Compatible with TTL outputs ...  $V_{IL} = 0.8V$  (Max.)  
 $V_{IH} = 2.0V$  (Min.)
- Wide Interfacing ability..... LSTTL, NMOS, CMOS
- Output Drive Capability ..... 15 LSTTL Loads
- Symmetrical Output Impedance...  $|I_{OH}| = I_{OL} = 6mA$  (Min.)
- Balanced Propagation Delays.....  $t_{pLH} \approx t_{pHL}$
- Pin and Function Compatible with 74LS540/541

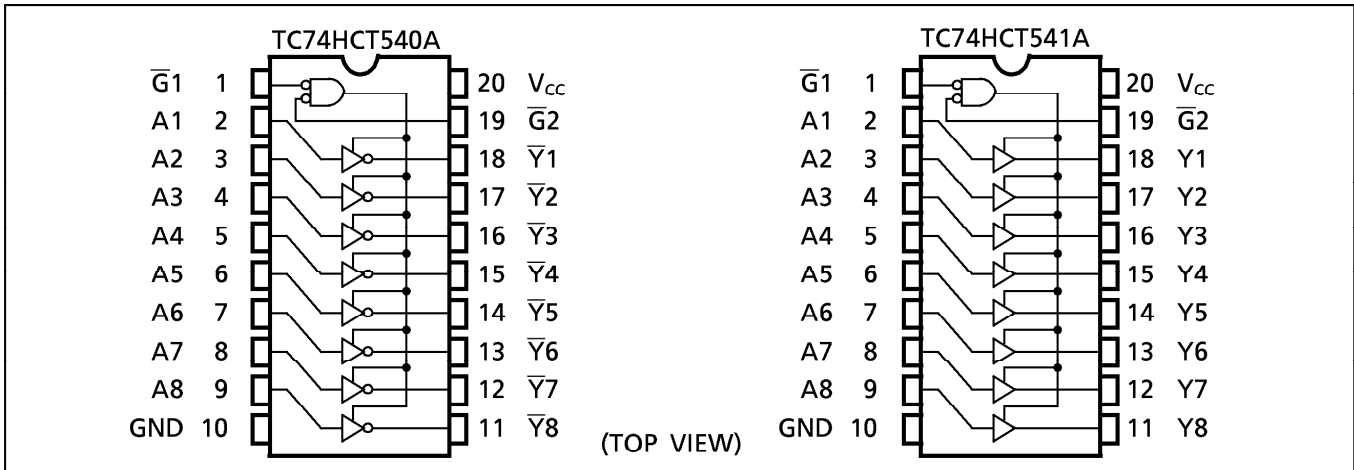


**TRUTH TABLE**

INPUTS			OUTPUTS	
$\bar{G}1$	$\bar{G}2$	$A_n$	$Y_n^*$	$\bar{Y}_n^*$
H	X	X	Z	Z
X	H	X	Z	Z
L	L	H	H	L
L	L	L	L	H

X : Don't Care  
 Z : High Impedance  
 \* :  $Y_n$  ..... HCT541A  
 $\bar{Y}_n$  ..... HCT540A

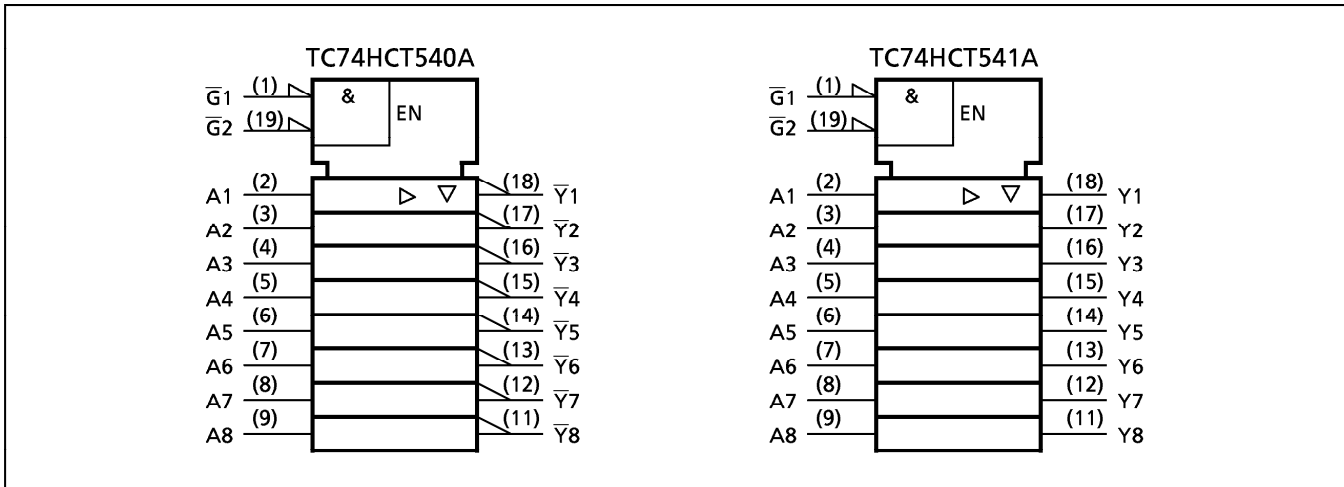
**PIN ASSIGNMENT**



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**IEC LOGIC SYMBOL**



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## ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	$V_{CC}$	$-0.5 \sim 7$	V
DC Input Voltage	$V_{IN}$	$-0.5 \sim V_{CC} + 0.5$	V
DC Output Voltage	$V_{OUT}$	$-0.5 \sim V_{CC} + 0.5$	V
Input Diode Current	$I_{IK}$	$\pm 20$	mA
Output Diode Current	$I_{OK}$	$\pm 20$	mA
DC Output Current	$I_{OUT}$	$\pm 35$	mA
DC $V_{CC}$ /Ground Current	$I_{CC}$	$\pm 75$	mA
Power Dissipation	$P_D$	500 (DIP)* / 180 (SOP)	mW
Storage Temperature	$T_{stg}$	$-65 \sim 150$	$^{\circ}\text{C}$

\*500mW in the range of  $T_a = -40^{\circ}\text{C} \sim 65^{\circ}\text{C}$ . From  $T_a = 65^{\circ}\text{C}$  to  $85^{\circ}\text{C}$  a derating factor of  $-10\text{mW}/^{\circ}\text{C}$  shall be applied until 300mW.

## RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage	$V_{CC}$	4.5~5.5	V
Input Voltage	$V_{IN}$	0~ $V_{CC}$	V
Output Voltage	$V_{OUT}$	0~ $V_{CC}$	V
Operating Temperature	$T_{opr}$	$-40 \sim 85$	$^{\circ}\text{C}$
Input Rise and Fall Time	$t_r, t_f$	0~500	ns

## DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION	$V_{CC}$ (V)	$T_a = 25^{\circ}\text{C}$			$T_a = -40 \sim 85^{\circ}\text{C}$		UNIT	
				MIN.	TYP.	MAX.	MIN.	MAX.		
High - Level Input Voltage	$V_{IH}$		4.5 § 5.5	2.0	—	—	2.0	—	V	
Low - Level Input Voltage	$V_{IL}$		4.5 § 5.5	—	—	0.8	—	0.8	V	
High - Level Output Voltage	$V_{OH}$	$V_{IN} = V_{IH}$ or $V_{IL}$	$I_{OH} = -20 \mu\text{A}$	4.5	4.4	4.5	—	4.4	—	V
			$I_{OH} = -6 \text{ mA}$	4.5	4.18	4.31	—	4.13	—	
Low - Level Output Voltage	$V_{OL}$	$V_{IN} = V_{IH}$ or $V_{IL}$	$I_{OL} = 20 \mu\text{A}$	4.5	—	0.0	0.1	—	0.1	V
			$I_{OL} = 6 \text{ mA}$	4.5	—	0.17	0.26	—	0.33	
3 - State Output Off - State Current	$I_{OZ}$	$V_{IN} = V_{IH}$ or $V_{IL}$ $V_{OUT} = V_{CC}$ or GND	5.5	—	—	$\pm 0.5$	—	$\pm 5.0$	$\mu\text{A}$	
Input Leakage Current	$I_{IN}$	$V_{IN} = V_{CC}$ or GND	5.5	—	—	$\pm 0.1$	—	$\pm 1.0$	$\mu\text{A}$	
Quiescent Supply Current	$I_{CC}$	$V_{IN} = V_{CC}$ or GND	5.5	—	—	4.0	—	40.0	$\mu\text{A}$	
	$I_C$	Per input: $V_{IN} = 0.5\text{V}$ or $2.4\text{V}$ Other input: $V_{CC}$ or GND	5.5	—	—	2.0	—	2.9	mA	

AC ELECTRICAL CHARACTERISTICS (Input  $t_r = t_f = 6\text{ns}$ )

PARAMETER	SYMBOL	TEST CONDITION	CL (pF)	V <sub>CC</sub> (V)	Ta = 25°C			Ta = -40~85°C		UNIT
					MIN.	TYP.	MAX.	MIN.	MAX.	
Output Transition Time	t <sub>TLH</sub>		50	4.5	—	7	12	—	15	ns
	t <sub>THL</sub>			4.5	—	6	11	—	14	
Propagation Delay Time (TC74HCT540A)	t <sub>pLH</sub>		50	4.5	—	12	20	—	25	
	t <sub>pHL</sub>			5.5	—	9	18	—	23	
	t <sub>pLH</sub>		150	4.5	—	17	26	—	33	
	t <sub>pHL</sub>			5.5	—	14	24	—	30	
Propagation Delay Time (TC74HCT541A)	t <sub>pLH</sub>		50	4.5	—	14	23	—	29	
	t <sub>pHL</sub>			5.5	—	11	21	—	27	
	t <sub>pLH</sub>		150	4.5	—	19	29	—	36	
	t <sub>pHL</sub>			5.5	—	16	27	—	33	
Output Enable time	t <sub>pZL</sub>	R <sub>L</sub> = 1kΩ	50	4.5	—	18	30	—	38	
	t <sub>pZH</sub>			5.5	—	16	27	—	35	
	t <sub>pZL</sub>		150	4.5	—	23	36	—	45	
	t <sub>pZH</sub>			5.5	—	21	33	—	41	
Output Disable time	t <sub>pLZ</sub> t <sub>pHZ</sub>	R <sub>L</sub> = 1kΩ	50	4.5 5.5	— —	18 16	30 27	— —	38 35	
Input Capacitance	C <sub>IN</sub>				—	5	10	—	10	pF
Output Capacitance	C <sub>OUT</sub>				—	10	—	—	—	
Power Dissipation Capacitance	C <sub>PD</sub> (1)	TC74HCT540A			—	35	—	—	—	
		TC74HCT541A			—	31	—	—	—	

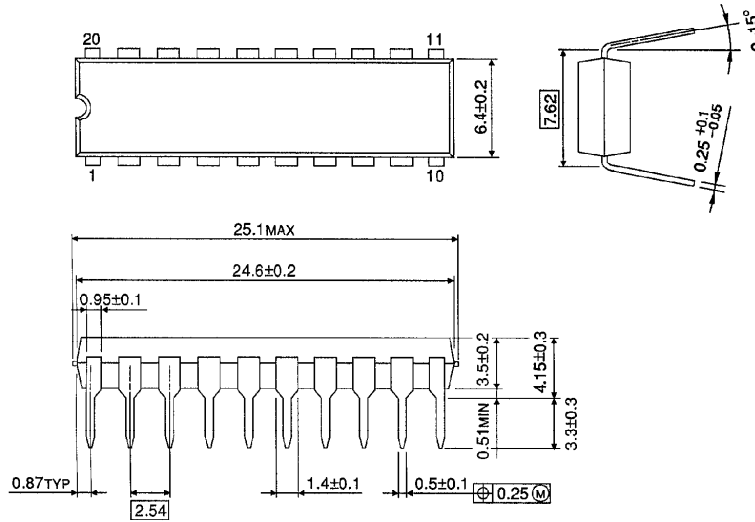
Note (1) C<sub>PD</sub> is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.

Average operating current can be obtained by the equation :

$$I_{CC}(\text{opr}) = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC} / 8 \text{ (per bit)}$$

**DIP 20PIN OUTLINE DRAWING (DIP20-P-300-2.54A)**

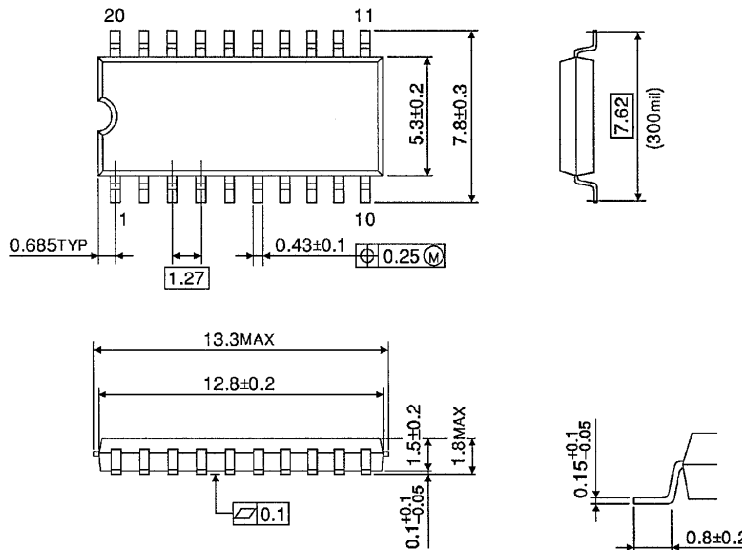
Unit in mm



Weight : 1.30g (Typ.)

**SOP 20PIN (200mil BODY) OUTLINE DRAWING (SOP20-P-300-1.27)**

Unit in mm

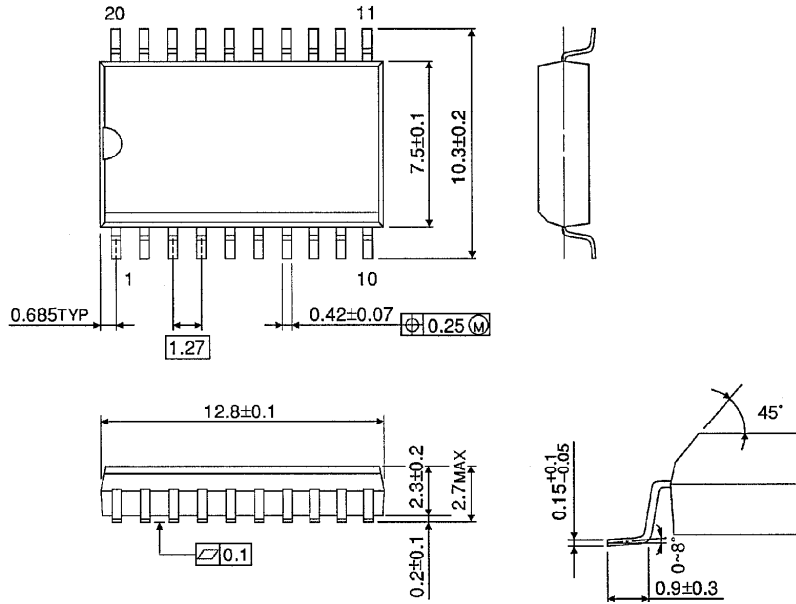


Weight : 0.22g (Typ.)

**SOP 20PIN (300mil BODY) OUTLINE DRAWING (SOL20-P-300-1.27)**

Unit in mm

(Note) This package is not available in Japan.



Weight : 0.46g (Typ.)