

## 8-BIT SINGLE-CHIP MICROCONTROLLER

## DESCRIPTION

The  $\mu$ PD78F0034A is a product of the  $\mu$ PD780034A Subseries in the 78K/0 Series, and is equivalent to the  $\mu$ PD780034A but with flash memory in place of internal ROM.

The  $\mu$ PD78F0034A incorporates flash memory, which can be programmed and erased while mounted on the board.

Detailed function descriptions are provided in the following user's manuals. Be sure to read them before designing.

$\mu$ PD780024A, 780034A, 780024AY, 780034AY Subseries User's Manual: Under preparation  
78K/0 Series User's Manual Instruction: U12326E

## FEATURES

- Pin-compatible with mask ROM versions (except  $V_{PP}$  pin)
- Flash memory: 32 Kbytes<sup>Note</sup>
- Internal high-speed RAM: 1024 bytes<sup>Note</sup>
- Supply voltage:  $V_{DD} = 1.8$  to 5.5 V

**Note** The flash memory and internal high-speed RAM capacities can be changed with the memory size switching register (IMS).

**Remark** For the differences between the flash memory and the mask ROM versions, refer to 1. DIFFERENCES BETWEEN  $\mu$ PD78F0034A AND MASK ROM VERSIONS.

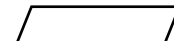
## ORDERING INFORMATION

Part Number	Package	Internal ROM
$\mu$ PD78F0034ACW	64-pin plastic shrink DIP (750 mils)	Flash memory
$\mu$ PD78F0034AGC-AB8	64-pin plastic QFP (14 × 14 mm)	Flash memory
$\mu$ PD78F0034AGK-8A8	64-pin plastic LQFP (12 × 12 mm)	Flash memory

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Not all devices/types available in every country. Please check with local NEC representative for availability and additional information.

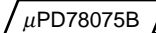
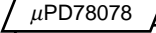
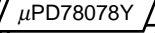
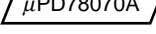
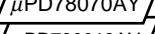
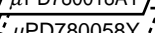
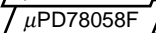
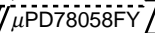
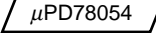
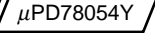
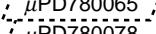
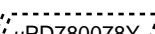
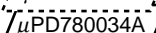
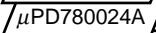
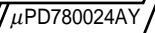
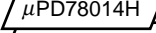
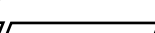
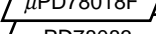
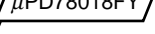
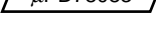


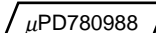

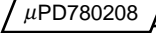
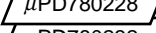
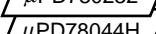
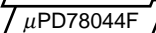

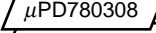
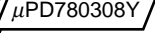
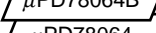
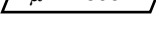
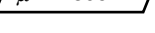
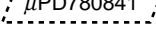
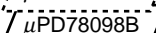
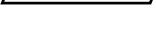
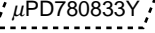

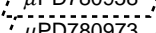
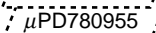

**78K/0 SERIES LINEUP**

The products in the 78K/0 Series are listed below. The names enclosed in boxes are subseries names.

 Products in mass-production

 Products under development

Y subseries products are compatible with I<sup>2</sup>C bus.

78K/0 Series	<b>Control</b>		
	100-pin		μPD78078 with reduced EMI noise
	100-pin	 	μPD78054 with timer and enhanced external interface function
	100-pin	 	ROM-less version of the μPD78078
	100-pin		μPD78078Y with enhanced serial I/O and select functions
	80-pin	 	μPD78054 with enhanced serial I/O and reduced EMI noise
	80-pin	 	μPD78054 with reduced EMI noise
	80-pin	 	μPD78018F with UART and D/A, and enhanced I/O
	80-pin		μPD780024A with expanded RAM
	64-pin	 	μPD780034A with timer and enhanced serial I/O
	64-pin	 	μPD780024A with enhanced A/D
	64-pin	 	μPD78018F with enhanced serial I/O
	64-pin		μPD78018F with reduced EMI noise
	64-pin	 	Basic subseries for control
	42/44-pin		On-chip UART and capable of low-voltage (1.8 V) operation
	<b>Inverter control</b>		
	64-pin		On-chip inverter control circuit and UART. EMI noise reduced products
	<b>FIP drive</b>		
100-pin		μPD78044F with enhanced I/O, FIP, C/D. Total display outputs: 53	
100-pin		μPD78044H with enhanced I/O, FIP, C/D. Total display outputs: 48	
80-pin		Panel control. On-chip FIP C/D. Total display outputs: 53	
80-pin		μPD78044F with N-ch open drain I/O. Total display outputs: 34	
80-pin		Basic subseries for FIP drive. Total display outputs: 34	
<b>LCD drive</b>			
100-pin	 	μPD78064 with enhanced SIO and expanded ROM and RAM	
100-pin		μPD78064 with reduced EMI noise	
100-pin	 	Basic subseries for LCD drive. On-chip UART	
<b>Call ID supported</b>			
80-pin		On-chip Call ID function and simple DTMF. EMI noise reduced products	
<b>Bus interface supported</b>			
100-pin		On-chip DCAN controller	
80-pin		μPD78054 with IEBus™ controller. EMI noise reduced products	
80-pin		On-chip DCAN/IEBus controller	
80-pin		On-chip J1850 (CLASS2) controller	
<b>Meter control</b>			
100-pin		For industrial meter control	
80-pin		On-chip controller/driver for automobile meter driving	
80-pin		Ultra low-power consumption and on-chip UART	

The major functional differences among subseries are listed below.

Function Subseries Name		ROM Capacity	Timer				8-Bit A/D	10-Bit A/D	8-Bit D/A	Serial Interface	I/O	V <sub>DD</sub> MIN. Value	External Expansion					
			8-Bit	16-Bit	Watch	WDT												
Control	μPD78075B	32 K to 40 K	4 ch	1 ch	1 ch	1 ch	8 ch	-	2 ch	3 ch (UART: 1 ch)	88	1.8 V	√					
	μPD78078	48 K to 60 K									61	2.7 V						
	μPD78070A	-																
	μPD780058	24 K to 60 K	2 ch	-	-	-	-	-	-	3 ch (time-division UART: 1 ch)	68	1.8 V						
	μPD78058F	48 K to 60 K								3 ch (UART: 1 ch)	69	2.7 V						
	μPD78054	16 K to 60 K									2.0 V							
	μPD780065	40 K to 48 K								4 ch (UART: 1 ch)	60	2.7 V						
	μPD780078	48 K to 60 K								2 ch	-	8 ch		3 ch (UART: 2 ch)	52	1.8 V		
	μPD780034A	8 K to 32 K								1 ch				3 ch (UART: 1 ch)	51			
	μPD780024A											8 ch		-				
	μPD78014H													2 ch	53			
	μPD78018F	8 K to 60 K															1 ch (UART: 1 ch)	33
μPD78083	8 K to 16 K									-	-							
Inverter control	μPD780988	16 K to 60 K	3 ch	<b>Note</b>	-	1 ch	-	8 ch	-	3 ch (UART: 2 ch)	47	4.0 V	√					
FIP control	μPD780208	32 K to 60 K	2 ch	1 ch	1 ch	1 ch	8 ch	-	-	2 ch	74	2.7 V	-					
	μPD780228	48 K to 60 K	3 ch	-	-					1 ch	72	4.5 V						
	μPD780232	16 K to 24 K					4 ch			2 ch	40							
	μPD78044H	32 K to 48 K	2 ch	1 ch	1 ch		8 ch			1 ch	68	2.7 V						
	μPD78044F	16 K to 40 K								2 ch								
LCD drive	μPD780308	48 K to 60 K	2 ch	1 ch	1 ch	1 ch	8 ch	-	-	3 ch (time-division UART: 1 ch)	57	2.0 V	-					
	μPD78064B	32 K								2 ch (UART: 1 ch)								
	μPD78064	16 K to 32 K																
Call ID supported	μPD780841	24 K to 32 K	2 ch	-	1 ch	1 ch	2 ch	-	-	2 ch (UART: 1 ch)	61	2.7 V	-					
Bus interface supported	μPD70948	60 K	2 ch	2 ch	1 ch	1 ch	8 ch	-	-	3 ch (UART: 1 ch)	79	4.0 V	√					
	μPD78098B	40 K to 60 K		1 ch					2 ch		69	2.7 V	-					
Meter control	μPD780958	48 K to 60 K	4 ch	2 ch	-	1 ch	-	-	-	2 ch (UART: 1 ch)	69	2.2 V	-					
	μPD780973	24 K to 32 K	3 ch	1 ch	1 ch		5 ch				56	4.5 V						
	μPD780955	40 K	6 ch		-		1 ch			2 ch (UART: 2 ch)	50	2.2 V						

**Note** 16-bit timer: 2 channels  
10-bit timer: 1 channel

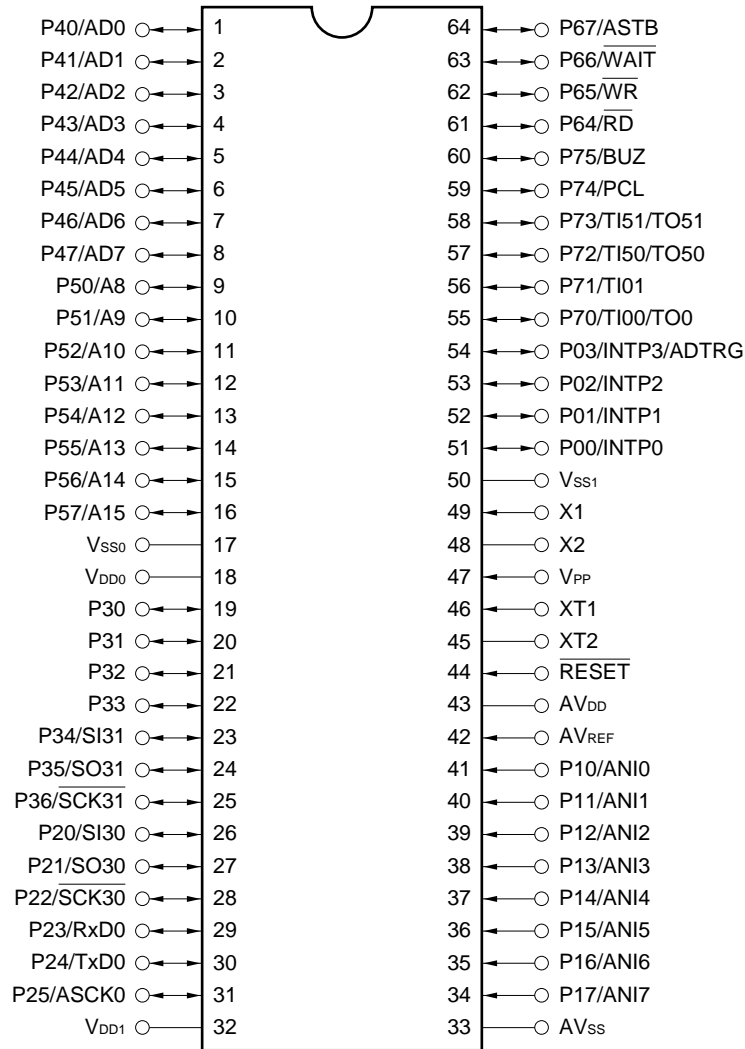
OVERVIEW OF FUNCTIONS

Item		Function
Internal memory	Flash memory	32 Kbytes <sup>Note</sup>
	High-speed RAM	1024 bytes <sup>Note</sup>
Memory space		64 Kbytes
General-purpose registers		8 bits × 32 registers (8 bits × 8 registers × 4 banks)
Minimum instruction execution time		On-chip minimum instruction execution time cycle modification function
	When main system clock selected	0.24 μs/0.48 μs/0.95 μs/1.91 μs/3.81 μs (@ 8.38-MHz operation)
	When subsystem clock selected	122 μs (@ 32.768-kHz operation)
Instruction set		<ul style="list-style-type: none"> <li>• 16-bit operation, multiply/divide (8 bits × 8 bits, 16 bits ÷ 8 bits)</li> <li>• Bit manipulation (set, reset, test, Boolean operation)</li> <li>• BCD adjust, etc.</li> </ul>
I/O ports		Total: 51 <ul style="list-style-type: none"> <li>• CMOS input: 8</li> <li>• CMOS I/O: 39</li> <li>• N-ch open drain I/O (5-V resistance): 4</li> </ul>
A/D converter		<ul style="list-style-type: none"> <li>• 10-bit resolution × 8 channels</li> <li>• Operable over a wide power supply voltage range: AV<sub>DD</sub> = 1.8 to 5.5 V</li> </ul>
Serial interface		<ul style="list-style-type: none"> <li>• UART mode: 1 channel</li> <li>• 3-wire serial I/O mode: 2 channels</li> </ul>
Timer		<ul style="list-style-type: none"> <li>• 16-bit timer/event counter: 1 channel</li> <li>• 8-bit timer/event counter: 2 channels</li> <li>• Watch timer: 1 channel</li> <li>• Watchdog timer: 1 channel</li> </ul>
Timer outputs		3 (8-bit PWM output capable: 2)
Clock output		65.5 kHz, 131 kHz, 262 kHz, 524 kHz, 1.05 MHz, 2.10 MHz, 4.19 MHz, 8.38 MHz (@ 8.38-MHz operation with main system clock) 32.768 kHz (@ 32.768-kHz operation with subsystem clock)
Buzzer output		1.02 kHz, 2.05 kHz, 4.10 kHz, 8.19 kHz (@ 8.38-MHz operation with main system clock)
Vectored interrupt sources	Maskable	Internal: 13 External: 5
	Non-maskable	Internal: 1
	Software	1
Test inputs		Internal: 1 External: 1
Supply voltage		V <sub>DD</sub> = 1.8 to 5.5 V
Operating ambient temperature		T <sub>A</sub> = -40 to +85°C
Package		<ul style="list-style-type: none"> <li>• 64-pin plastic shrink DIP (750 mils)</li> <li>• 64-pin plastic QFP (14 × 14 mm)</li> <li>• 64-pin plastic LQFP (12 × 12 mm)</li> </ul>

**Note** The capacities of the flash memory and the internal high-speed RAM can be changed with the memory size switching register (IMS).

**PIN CONFIGURATION (TOP VIEW)**

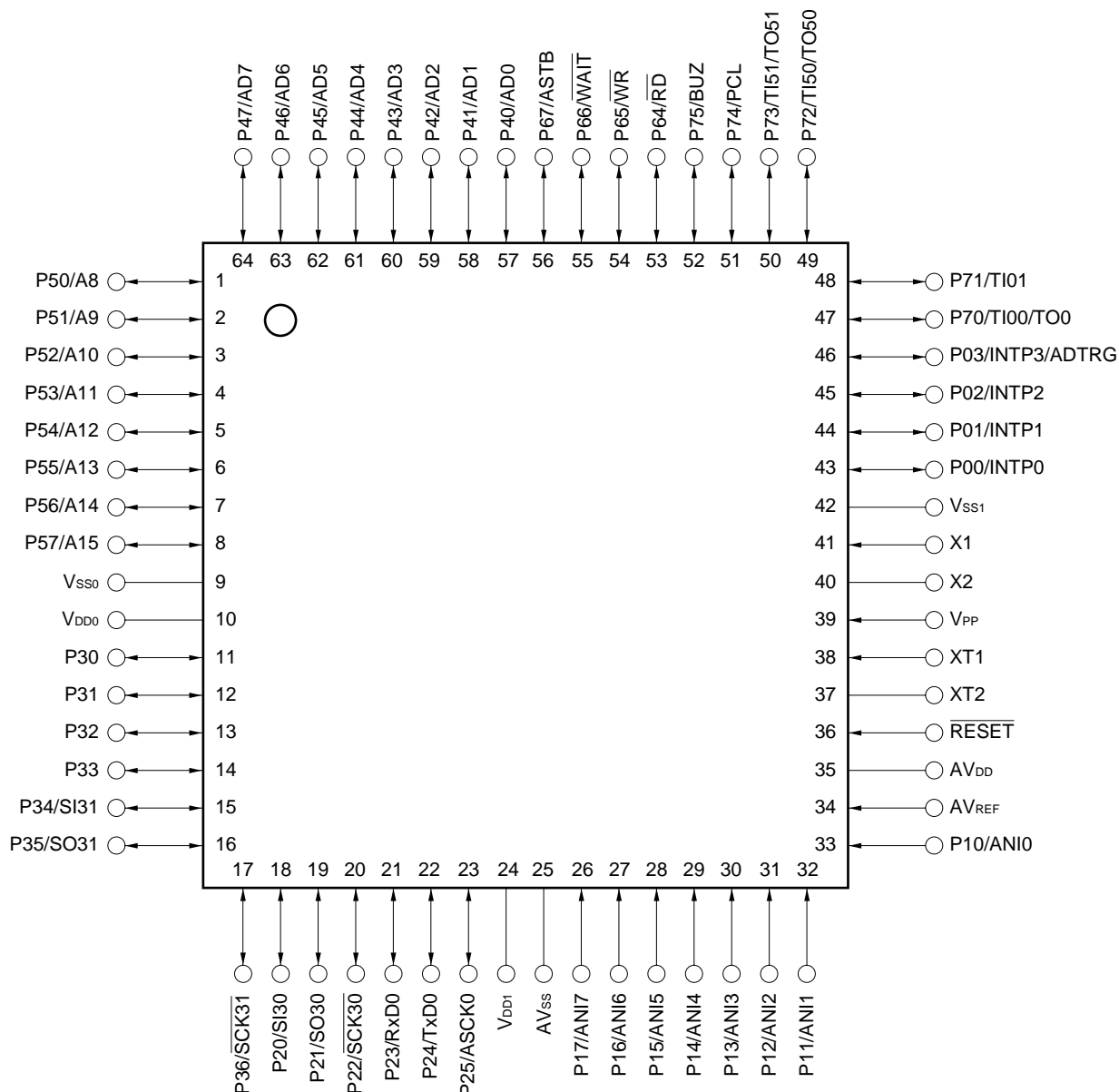
- 64-pin plastic shrink DIP (750 mils)  
μPD78F0034ACW



- Cautions**
1. Connect the VPP pin directly to VSS0 or VSS1 in normal operation mode.
  2. Connect the AVSS pin to VSS0.

**Remark** When the μPD78F0034A is used in application fields that require reduction of the noise generated from inside the microcontroller, the implementation of noise reduction measures, such as supplying voltage to VDD0 and VDD1 individually and connecting VSS0 and VSS1 to different ground lines, is recommended.

- 64-pin plastic QFP (14 × 14 mm)  
μPD78F0034AGC-AB8
- 64-pin plastic LQFP (12 × 12 mm)  
μPD78F0034AGK-8A8

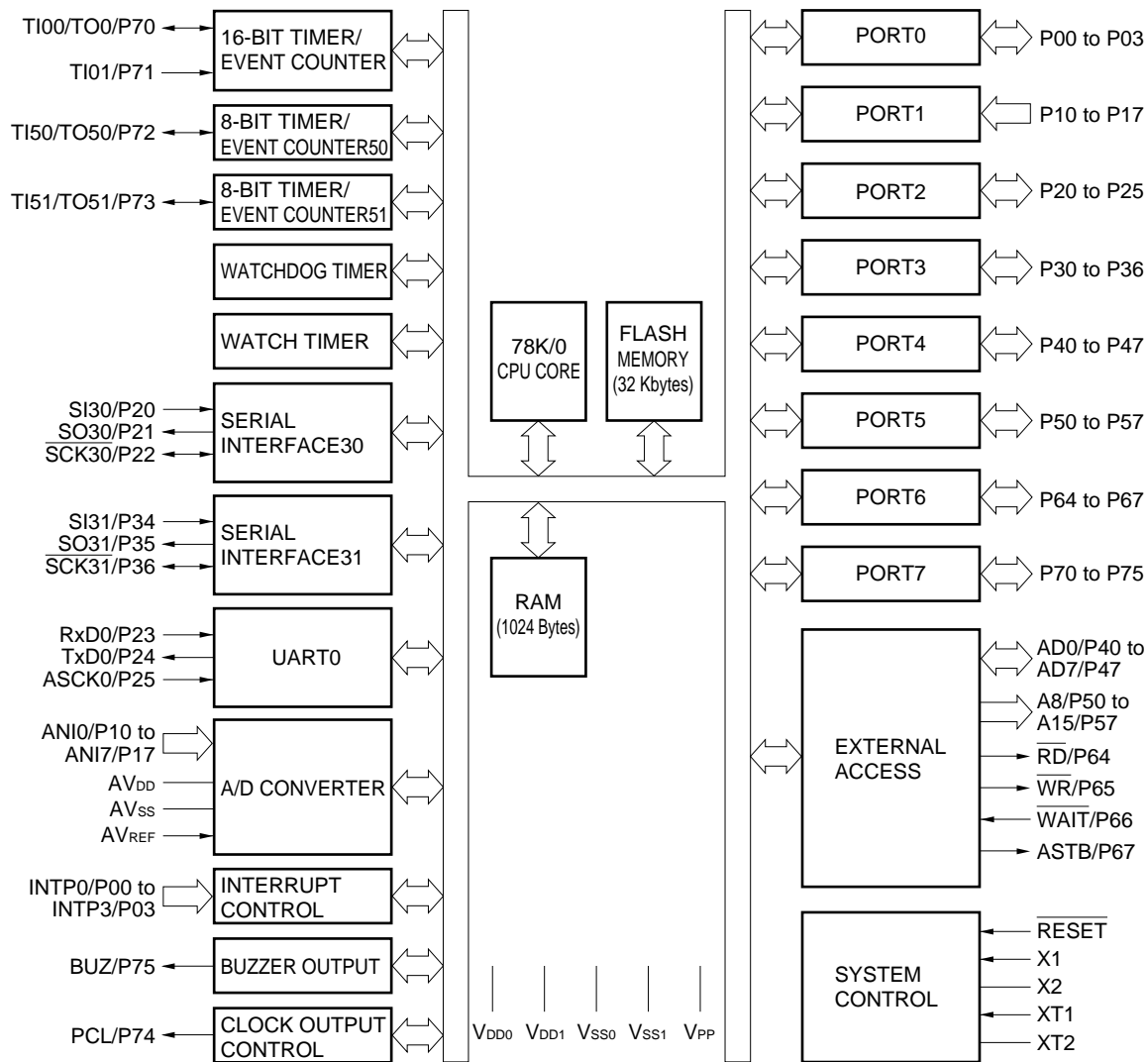


- Cautions**
1. Connect the V<sub>PP</sub> pin directly to V<sub>SS0</sub> or V<sub>SS1</sub> in normal operation mode.
  2. Connect the AV<sub>SS</sub> pin to V<sub>SS0</sub>.

**Remark** When the μPD78F0034A is used in application fields that require reduction of the noise generated from inside the microcontroller, the implementation of noise reduction measures, such as supplying voltage to V<sub>DD0</sub> and V<sub>DD1</sub> individually and connecting V<sub>SS0</sub> and V<sub>SS1</sub> to different ground lines, is recommended.

A8 to A15:	Address Bus	P70 to P75:	Port 7
AD0 to AD7:	Address/Data Bus	PCL:	Programmable Clock
ADTRG:	AD Trigger Input	$\overline{\text{RD}}$ :	Read Strobe
ANI0 to ANI7:	Analog Input	$\overline{\text{RESET}}$ :	Reset
ASCK0:	Asynchronous Serial Clock	RxD0:	Receive Data
ASTB:	Address Strobe	$\overline{\text{SCK30}}$ , $\overline{\text{SCK31}}$ :	Serial Clock
AV <sub>DD</sub> :	Analog Power Supply	SI30, SI31:	Serial Input
AV <sub>REF</sub> :	Analog Reference Voltage	SO30, SO31:	Serial Output
AV <sub>SS</sub> :	Analog Ground	TI00, TI01, TI50, TI51:	Timer Input
BUZ:	Buzzer Clock	TO0, TO50, TO51:	Timer Output
INTP0 to INTP3:	External Interrupt Input	TxD0:	Transmit Data
P00 to P03:	Port 0	V <sub>DD0</sub> , V <sub>DD1</sub> :	Power Supply
P10 to P17:	Port 1	V <sub>PP</sub> :	Programming Power Supply
P20 to P25:	Port 2	V <sub>SS0</sub> , V <sub>SS1</sub> :	Ground
P30 to P36:	Port 3	$\overline{\text{WAIT}}$ :	Wait
P40 to P47:	Port 4	$\overline{\text{WR}}$ :	Write Strobe
P50 to P57:	Port 5	X1, X2:	Crystal (Main System Clock)
P64 to P67:	Port 6	XT1, XT2:	Crystal (Subsystem Clock)

BLOCK DIAGRAM





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1. DIFFERENCES BETWEEN μPD78F0034A AND MASK ROM VERSIONS

The μPD78F0034A is a product provided with a flash memory which enables writing, erasing, and rewriting of programs with device mounted on the target system.

The functions of the μPD78F0034A (except the functions specified for flash memory) can be made the same as those of the mask ROM versions by setting the memory size switching register (IMS).

Table 1-1 shows the differences between the flash memory (μPD78F0034A) and the mask ROM versions.

Table 1-1. Differences Between μPD78F0034A and Mask ROM Versions

Item	μPD78F0034A	Mask ROM Versions	
		μPD780034A Subseries	μPD780024A Subseries <sup>Note</sup>
Internal ROM structure	Flash memory	Mask ROM	
Internal ROM capacity	32 Kbytes	μPD780031A: 8 Kbytes μPD780032A: 16 Kbytes μPD780033A: 24 Kbytes μPD780034A: 32 Kbytes	μPD780021A: 8 Kbytes μPD780022A: 16 Kbytes μPD780023A: 24 Kbytes μPD780024A: 32 Kbytes
Internal high-speed RAM capacity	1024 bytes	μPD780031A: 512 bytes μPD780032A: 512 bytes μPD780033A: 1024 bytes μPD780034A: 1024 bytes	μPD780021A: 512 bytes μPD780022A: 512 bytes μPD780023A: 1024 bytes μPD780024A: 1024 bytes
A/D converter resolution	10 bits		8 bits
Mask option specification of on-chip pull-up resistor for pins P30 to P33	Not available	Available	
IC pin	Not provided	Provided	
V <sub>PP</sub> pin	Provided	Not provided	
Electrical specifications, recommended soldering conditions	Refer to the data sheet of individual products.		

**Note** The μPD78F0034A can be used as the flash memory version of the μPD780024A Subseries.

**Caution** There are differences in noise immunity and noise radiation between the flash memory and mask ROM versions. When pre-producing an application set with the flash memory version and then mass producing it with the mask ROM version, be sure to conduct sufficient evaluations on the commercial samples (CS) (not engineering samples (ES)) of the mask ROM versions.

2. PIN FUNCTIONS

2.1 Port Pins (1/2)

Pin Name	I/O	Function		After Reset	Alternate Function	
P00	I/O	Port 0 4-bit input/output port. Input/output can be specified in 1-bit units. An on-chip pull-up resistor can be specified by means of software.		Input	INTP0	
P01					INTP1	
P02					INTP2	
P03					INTP3/ADTRG	
P10 to P17	Input	Port 1 8-bit input only port.		Input	ANI0 to ANI7	
P20	I/O	Port 2 6-bit input/output port. Input/output can be specified in 1-bit units. An on-chip pull-up resistor can be specified by means of software.		Input	SI30	
P21					SO30	
P22					SCK30	
P23					RxD0	
P24					TxD0	
P25					ASCK0	
P30	I/O	Port 3 7-bit input/output port. Input/output can be specified in 1-bit units.	N-ch open drain input/output port. LEDs can be driven directly.	Input	—	
P31					An on-chip pull-up resistor can be specified by means of software.	SI31
P32						SO31
P33		SCK31				
P34						
P35						
P36						
P40 to P47	I/O	Port 4 8-bit input/output port. Input/output can be specified in 1-bit units. An on-chip pull-up resistor can be specified by means of software. Interrupt request flag KRIF is set to 1 by falling edge detection.		Input	AD0 to AD7	
P50 to P57	I/O	Port 5 8-bit input/output port. LEDs can be driven directly. Input/output can be specified in 1-bit units. An on-chip pull-up resistor can be specified by means of software.		Input	A8 to A15	
P64	I/O	Port 6 4-bit input/output port. Input/output can be specified in 1-bit units. An on-chip pull-up resistor can be specified by means of software.		Input	$\overline{RD}$	
P65					$\overline{WR}$	
P66					$\overline{WAIT}$	
P67					ASTB	

2.1 Port Pins (2/2)

Pin Name	I/O	Function	After Reset	Alternate Function
P70	I/O	Port 7 6-bit input/output port. Input/output can be specified in 1-bit units. An on-chip pull-up resistor can be specified by means of software.	Input	TI00/TO0
P71				TI01
P72				TI50/TO50
P73				TI51/TO51
P74				PCL
P75				BUZ

2.2 Non-Port Pins (1/2)

Pin Name	I/O	Function	After Reset	Alternate Function
INTP0	Input	External interrupt request input by which the valid edge (rising edge, falling edge, or both rising and falling edges) can be specified.	Input	P00
INTP1				P01
INTP2				P02
INTP3				P03/ADTRG
SI30	Input	Serial interface serial data input.	Input	P20
SI31				P34
SO30	Output	Serial interface serial data output.	Input	P21
SO31				P35
$\overline{\text{SCK30}}$	I/O	Serial interface serial clock input/output.	Input	P22
$\overline{\text{SCK31}}$				P36
RxD0	Input	Serial data input for asynchronous serial interface.	Input	P23
TxD0	Output	Serial data output for asynchronous serial interface.	Input	P24
ASCK0	Input	Serial clock input for asynchronous serial interface.	Input	P25
TI00	Input	External count clock input to 16-bit timer (TM0). Capture trigger signal input to TM0 capture register (CR01).	Input	P70/TO0
TI01		Capture trigger signal input to TM0 capture register (CR00).		P71
TI50		External count clock input to 8-bit timer (TM50).		P72/TO50
TI51		External count clock input to 8-bit timer (TM51).		P73/TO51
TO0	Output	16-bit timer (TM0) output.	Input	P70/TO0
TO50		8-bit timer (TM50) output (shared with 8-bit PWM output).	Input	P72/TO50
TO51		8-bit timer (TM51) output (shared with 8-bit PWM output).		P73/TO51
PCL	Output	Clock output (for trimming of main system clock and subsystem clock).	Input	P74
BUZ	Output	Buzzer output.	Input	P75
AD0 to AD7	I/O	Lower address/data bus for extending memory externally.	Input	P40 to P47
A8 to A15	Output	Higher address bus for extending memory externally.	Input	P50 to P57
$\overline{\text{RD}}$	Output	Strobe signal output for read operation of external memory.	Input	P64
$\overline{\text{WR}}$		Strobe signal output for write operation of external memory.		P65
$\overline{\text{WAIT}}$	Input	Inserting wait for accessing external memory.	Input	P66
ASTB	Output	Strobe output which externally latches address information output to ports 4 and 5 to access external memory.	Input	P67

2.2 Non-Port Pins (2/2)

Pin Name	I/O	Function	After Reset	Alternate Function
ANI0 to ANI7	Input	A/D converter analog input.	Input	P10 to P17
ADTRG	Input	A/D converter trigger signal input.	Input	P03/INTP3
AV <sub>REF</sub>	Input	A/D converter reference voltage input.	—	—
AV <sub>DD</sub>	—	A/D converter analog power supply. Set the voltage equal to V <sub>DD0</sub> or V <sub>DD1</sub> .	—	—
AV <sub>SS</sub>	—	A/D converter ground potential. Set the voltage equal to V <sub>SS0</sub> or V <sub>SS1</sub> .	—	—
RESET	Input	System reset input.	—	—
X1	Input	Connecting crystal resonator for main system clock oscillation.	—	—
X2	—		—	—
XT1	Input	Connecting crystal resonator for subsystem clock oscillation.	—	—
XT2	—		—	—
V <sub>DD0</sub>	—	Positive power supply voltage for ports.	—	—
V <sub>SS0</sub>	—	Ground potential of ports.	—	—
V <sub>DD1</sub>	—	Positive power supply (except ports).	—	—
V <sub>SS1</sub>	—	Ground potential (except ports).	—	—
V <sub>PP</sub>	—	Applying high-voltage for program write/verify. Connect directly to V <sub>SS0</sub> or V <sub>SS1</sub> in normal operation mode.	—	—

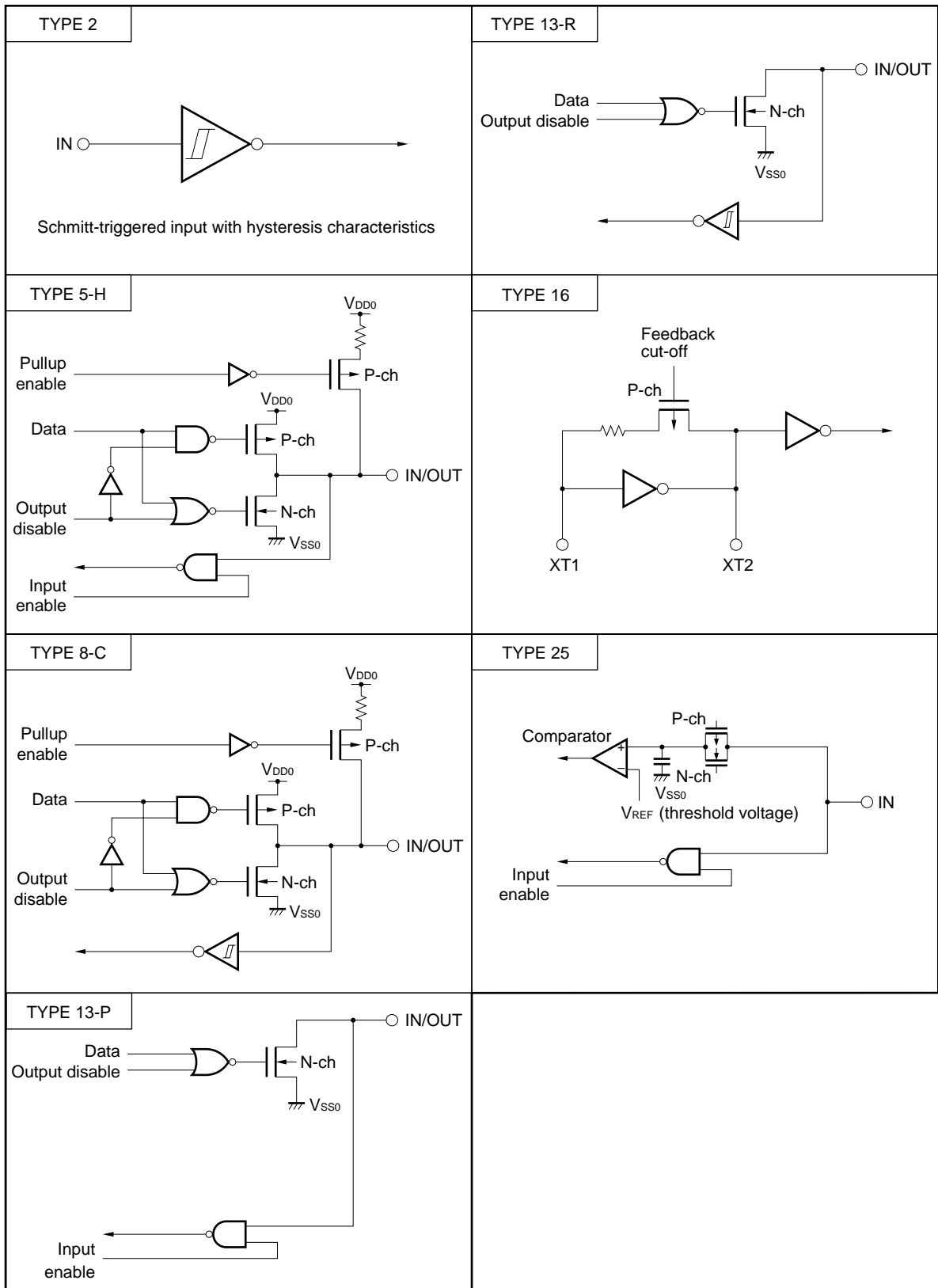
2.3 Pin I/O Circuits and Recommended Connection of Unused Pins

The input/output circuit type of each pin and recommended connection of unused pins are shown in Table 2-1. For the input/output configuration of each type, refer to Figure 2-1 .

Table 2-1. Types of Pin Input/Output Circuits

Pin Name	Input/Output Circuit Type	I/O	Recommended Connection of Unused Pins		
P00/INTP0	8-C	Input	Independently connect to V <sub>SS0</sub> via a resistor.		
P01/INTP1					
P02/INTP2					
P03/INTP3/ADTRG					
P10/ANI0 to P17/ANI7	25	Input	Independently connect to V <sub>DD0</sub> or V <sub>SS0</sub> via a resistor.		
P20/SI30	8-C	Input/output			
P21/SO30	5-H				
P22/SCK30	8-C				
P23/RxD0					
P24/TxD0	5-H				
P25/ASCK0	8-C				
P30, P31	13-P			Input/output	Independently connect to V <sub>DD0</sub> via a resistor.
P32, P33	13-R				
P34/SI31	8-C				Independently connect to V <sub>DD0</sub> or V <sub>SS0</sub> via a resistor.
P35/SO31	5-H				
P36/SCK31	8-C				
P40/AD0 to P47/AD7	5-H	Input/output	Independently connect to V <sub>DD0</sub> via a resistor.		
P50/A8 to P57/A15	5-H	Input/output	Independently connect to V <sub>DD0</sub> or V <sub>SS0</sub> via a resistor.		
P64/RD		Input/output			
P65/WR					
P66/WAIT					
P67/ASTB					
P70/TI00/TO0				8-C	
P71/TI01					
P72/TI50/TO50					
P73/TI51/TO51					
P74/PCL				5-H	
P75/BUZ					
RESET	2	Input	—		
XT1	16			Connect to V <sub>DD0</sub> .	
XT2			—	Leave open.	
AV <sub>DD</sub>	—		Connect to V <sub>DD0</sub> .		
AV <sub>REF</sub>			Connect to V <sub>SS0</sub> .		
AV <sub>SS</sub>					
V <sub>PP</sub>			Connect directly to V <sub>SS0</sub> or V <sub>SS1</sub> .		

Figure 2-1. Pin Input/Output Circuits



### 3. MEMORY SIZE SWITCHING REGISTER (IMS)

IMS is a register that is set by software and is used to specify a part of the internal memory that is not to be used. By setting IMS, the internal memory of the μPD78F0034A can be mapped identically to that of a mask ROM version. IMS is set with an 8-bit memory manipulation instruction.

RESET input sets the IMS to CFH.

**Caution** The initial value of IMS is setting disabled (CFH). Be sure to set C8H or the value of the target mask ROM version at the moment of initial setting.

Figure 3-1. Format of Memory Size Switching Register

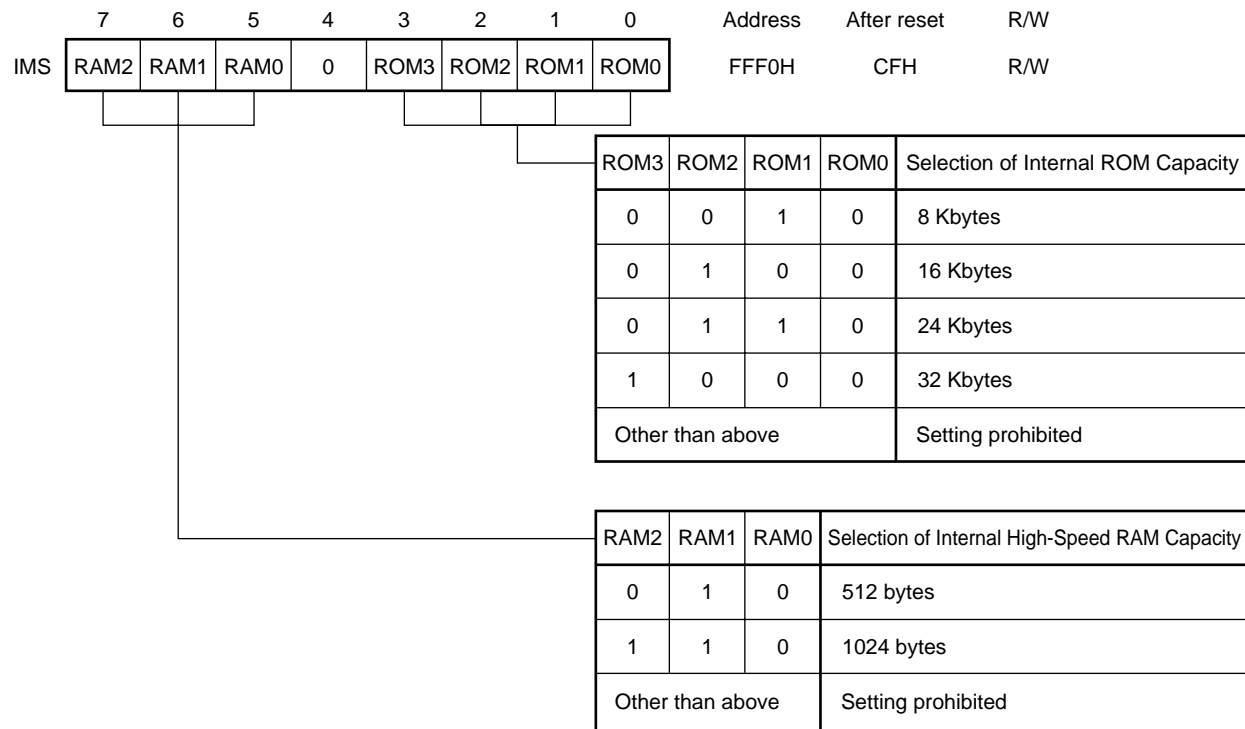


Table 3-1 shows the IMS set value to make the memory mapping the same as those of mask ROM versions.

Table 3-1. Set Value of Memory Size Switching Register

Target Mask ROM Versions	IMS Set Value
μPD780031A	42H
μPD780032A	44H
μPD780033A	C6H
μPD780034A	C8H



#### 4. FLASH MEMORY PROGRAMMING

Writing to flash memory can be performed without removing the memory from the target system (on board programming). Writing is performed with the dedicated flash programmer (Flashpro II (model No.: FL-PR2) or Flashpro III (model No.: FL-PR3 and PG-FP3)) connected to the host machine and the target system.

Writing to flash memory can also be performed using flash memory writing adapter connected to Flashpro II or Flashpro III.

**Remark** FL-PR2 and FL-PR3 are products of Naito Densai Machida Mfg. Co., Ltd.

##### 4.1 Selection of Communication Mode

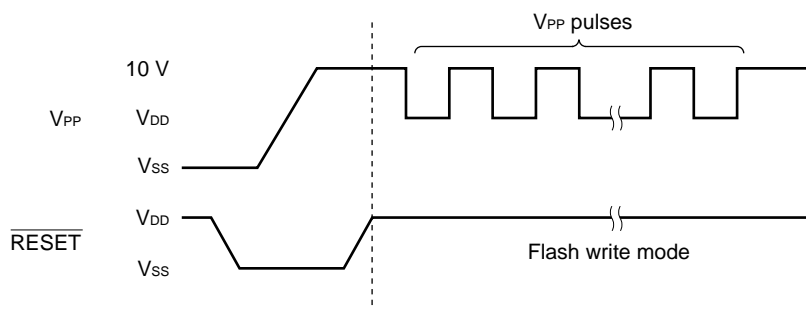
Writing to a flash memory is performed using Flashpro II or Flashpro III in a serial communication. Select one of the communication modes in Table 4-1. The selection of the communication mode is made by using the format shown in Figure 4-1. Each communication mode is selected by the number of  $V_{PP}$  pulses shown in Table 4-1.

**Table 4-1. List of Communication Mode**

Communication Mode	Channels	Used Pin	$V_{PP}$ Pulses
3-wire serial I/O	2	SI30/P20 SO30/P21 SCK30/P22	0
		SI31/P34 SO31/P35 SCK31/P36	1
UART	1	RxD0/P23 TxD0/P24	8
Pseudo 3-wire serial I/O	1	P72/TI50/TO50 (serial clock input) P71/TI01 (serial data output) P70/TI00/TO0 (serial data input)	12

**Caution** Be sure to select a communication mode using the number of  $V_{PP}$  pulses shown in Table 4-1.

**Figure 4-1. Format of Communication Mode Selection**



### 4.2 Flash Memory Programming Functions

Operations such as writing to flash memory are performed by various command/data transmission and reception operations according to the selected communication mode. Table 4-2 shows major functions of flash memory programming.

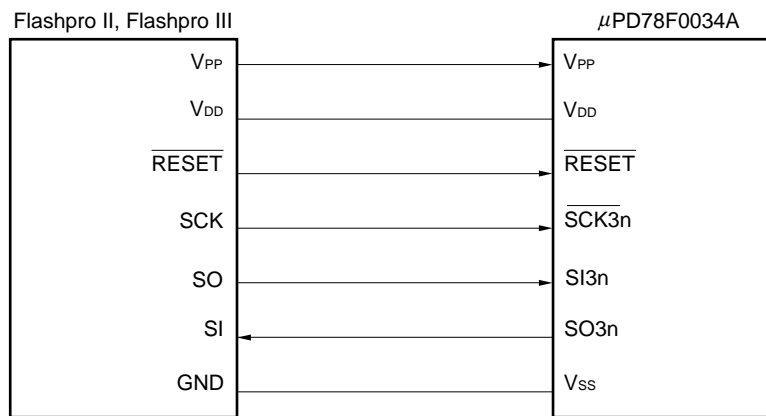
**Table 4-2. Major Functions of Flash Memory Programming**

Function	Description
Reset	Used to stop write operation and detect transmission cycle.
Batch verify	Compares the entire memory contents with the input data.
Batch erase	Erases the entire memory contents.
Batch blank check	Checks the deletion status of the entire memory.
High-speed write	Performs write to the flash memory based on the write start address and the number of data to be written (number of bytes).
Continuous write	Performs continuous write based on the information input with high-speed write operation.
Status	Used to confirm the current operating mode and operation end.
Oscillation frequency setting	Sets the frequency of the resonator.
Erase time setting	Sets the memory erase time.
Silicon signature read	Outputs the device name and memory capacity, and device block information.

### 4.3 Connection of Flashpro II and Flashpro III

The connection of Flashpro II or Flashpro III and the μPD78F0034A differs according to the communication mode (3-wire serial I/O, UART, and pseudo 3-wire serial I/O). The connection for each communication mode is shown in Figures 4-2, 4-3, and 4-4, respectively.

**Figure 4-2. Connection of Flashpro II or Flashpro III for 3-Wire Serial I/O Mode**



n = 0, 1

Figure 4-3. Connection of Flashpro II or Flashpro III for UART Mode

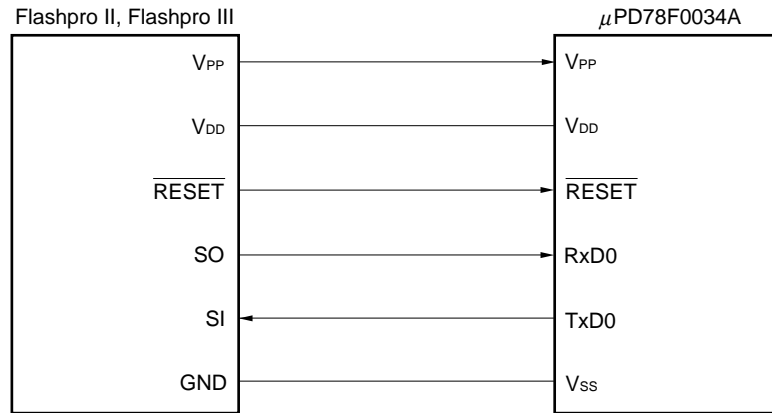
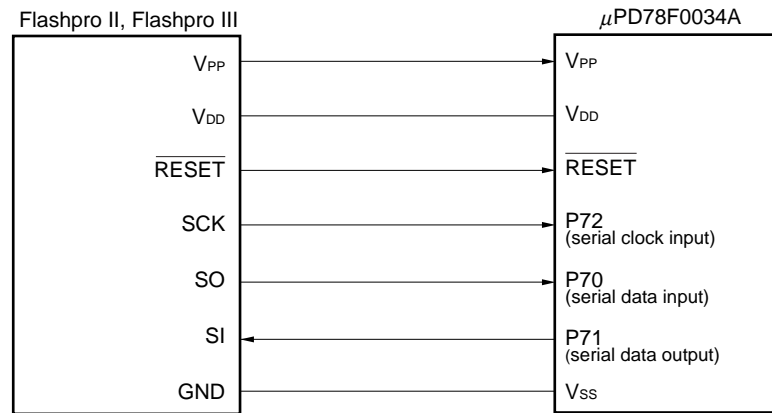


Figure 4-4. Connection of Flashpro II or Flashpro III for Pseudo 3-Wire Serial I/O Mode



## 5. ELECTRICAL SPECIFICATIONS

Absolute Maximum Ratings ( $T_A = 25^\circ\text{C}$ )

Parameter	Symbol	Test Conditions		Ratings	Unit
Supply voltage	$V_{DD}$			-0.3 to +6.5	V
	$V_{PP}$			-0.3 to +10.5	V
	$AV_{DD}$			-0.3 to $V_{DD} + 0.3$ <sup>Note</sup>	V
	$AV_{REF}$			-0.3 to $V_{DD} + 0.3$ <sup>Note</sup>	V
	$AV_{SS}$			-0.3 to +0.3	V
Input voltage	$V_{I1}$	P00 to P03, P10 to P17, P20 to P25, P34 to P36, P40 to P47, P50 to P57, P64 to P67, P70 to P75, X1, X2, XT1, XT2, RESET		-0.3 to $V_{DD} + 0.3$ <sup>Note</sup>	V
	$V_{I2}$	P30 to P33	N-ch open drain	-0.3 to +6.5	V
Output voltage	$V_O$			-0.3 to $V_{DD} + 0.3$ <sup>Note</sup>	V
Analog input voltage	$V_{AN}$	P10 to P17	Analog input pin	$AV_{SS} - 0.3$ to $AV_{REF} + 0.3$ <sup>Note</sup> and -0.3 to $V_{DD} + 0.3$ <sup>Note</sup>	V
Output current, high	$I_{OH}$	Per pin		-10	mA
		Total for P00 to P03, P40 to P47, P50 to P57, P64 to P67, P70 to P75		-15	mA
		Total for P20 to P25, P30 to P36		-15	mA
Output current, low	$I_{OL}$	Per pin for P00 to P03, P20 to P25, P34 to P36, P40 to P47, P64 to P67, P70 to P75		20	mA
		Per pin for P30 to P33, P50 to P57		30	mA
		Total for P00 to P03, P40 to P47, P64 to P67, P70 to P75		50	mA
		Total for P20 to P25		20	mA
		Total for P30 to P36		100	mA
		Total for P50 to P57		100	mA
Operating ambient temperature	$T_A$			-40 to +85	$^\circ\text{C}$
Storage temperature	$T_{stg}$			-40 to +125	$^\circ\text{C}$

**Note** The rating should be 6.5 V or less.

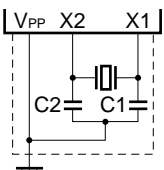
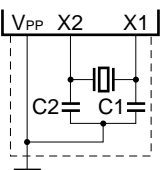
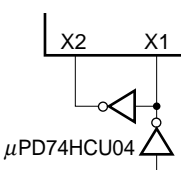
**Caution** Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

**Capacitance (T<sub>A</sub> = 25°C, V<sub>DD</sub> = V<sub>SS</sub> = 0 V)**

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit	
Input capacitance	C <sub>IN</sub>	f = 1 MHz Pins other than measured pins returned to 0 V.			15	pF	
I/O capacitance	C <sub>IO</sub>	f = 1 MHz Pins other than measured pins returned to 0 V.	P00 to P03, P20 to P25, P34 to P36, P40 to P47, P50 to P57, P64 to P67, P70 to P75,			15	pF
			P30 to P33			20	pF

**Remark** Unless specified otherwise, the characteristics of alternate-function pins are the same as those of port pins.

**Main System Clock Oscillation Circuit Characteristics (T<sub>A</sub> = -40 to 85°C, V<sub>DD</sub> = 1.8 to 5.5 V)**

Resonator	Recommended Circuit	Parameter	Test Conditions	MIN.	TYP.	MAX.	Unit
Ceramic resonator		Oscillation frequency (f <sub>x</sub> ) <sup>Note 1</sup>	V <sub>DD</sub> = 4.0 to 5.5 V	1.0		8.38	MHz
		Oscillation stabilization time <sup>Note 2</sup>	After V <sub>DD</sub> reaches oscillation voltage range MIN.			4	
Crystal resonator		Oscillation frequency (f <sub>x</sub> ) <sup>Note 1</sup>	V <sub>DD</sub> = 4.0 to 5.5 V	1.0		8.38	MHz
		Oscillation stabilization time <sup>Note 2</sup>	V <sub>DD</sub> = 4.0 to 5.5 V			10	
External clock		X1 input frequency (f <sub>x</sub> ) <sup>Note 1</sup>	V <sub>DD</sub> = 4.0 to 5.5 V	1.0		8.38	MHz
		X1 input high-/low-level width (t <sub>xH</sub> , t <sub>xL</sub> )	V <sub>DD</sub> = 4.0 to 5.5 V	50		500	
				85		500	

**Notes** 1. Indicates only oscillation circuit characteristics. Refer to **AC Characteristics** for instruction execution time.

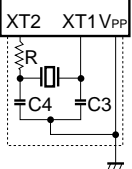
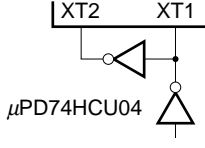
2. Time required to stabilize oscillation after reset or STOP mode release.

**Cautions** 1. When using the main system clock oscillator, wire as follows in the area enclosed by the broken lines in the above figures to avoid an adverse effect from wiring capacitance.

- Keep the wiring length as short as possible.
- Do not cross the wiring with the other signal lines.
- Do not route the wiring near a signal line through which a high fluctuating current flows.
- Always keep the ground point of the oscillator capacitor the same potential as V<sub>SS1</sub>.
- Do not ground the capacitor to a ground pattern through which a high current flows.
- Do not fetch signals from the oscillator.

2. When the main system clock is stopped and the system is operated by the subsystem clock, the subsystem clock should be switched again to the main system clock after the oscillation stabilization time is secured by the program.

Subsystem Clock Oscillation Circuit Characteristics (T<sub>A</sub> = -40 to +85°C, V<sub>DD</sub> = 1.8 to 5.5 V)

Resonator	Recommended Circuit	Parameter	Test Conditions	MIN.	TYP.	MAX.	Unit
Crystal resonator		Oscillation frequency (f <sub>X1</sub> ) <sup>Note 1</sup>		32	32.768	35	kHz
		Oscillation stabilization time <sup>Note 2</sup>	V <sub>DD</sub> = 4.0 to 5.5 V		1.2	2	s
External clock		X1 input frequency (f <sub>X1</sub> ) <sup>Note 1</sup>		32		38.5	kHz
		X1 input high-/low-level width (t <sub>XTH</sub> , t <sub>XTL</sub> )		5		15	μs

**Notes** 1. Indicates only oscillation circuit characteristics. Refer to **AC Characteristics** for instruction execution time.

2. Time required to stabilize oscillation after V<sub>DD</sub> reaches oscillator voltage MIN.

**Cautions** 1. When using the subsystem clock oscillator, wire as follows in the area enclosed by the broken line in the above figures to avoid an adverse effect from wiring capacitance.

- Keep the wiring length as short as possible.
- Do not cross the wiring with the other signal lines.
- Do not route the wiring near a signal line through which a high fluctuating current flows.
- Always keep the ground point of the oscillator to the same potential as V<sub>SS1</sub>.
- Do not ground the capacitor to a ground pattern in which a high current flows.
- Do not fetch signals from the oscillator.

2. The subsystem clock oscillator is designed as a low-amplitude circuit for reducing current consumption, and is more prone to malfunction due to noise than the main system clock oscillator. Particular care is therefore required with the wiring method when the subsystem clock is used.

Recommended Oscillator Constant

Main System Clock: Ceramic Resonator (T<sub>A</sub> = -40 to +85°C)

Manufacturer	Part Number	Frequency (MHz)	Recommended Circuit Constant		Oscillation Voltage Range	
			C1 (pF)	C2 (pF)	MIN. (V)	MAX. (V)
Murata Mfg. Co., Ltd.	CSB1000J	1.00	100	100	1.9	5.5
	CSA2.00MG040	2.00	100	100	2.0	5.5
	CST2.00MG040	2.00	On-chip	On-chip	2.0	5.5
	CSA3.58MG	3.58	30	30	2.0	5.5
	CST3.58MGW	3.58	On-chip	On-chip	2.0	5.5
	CSA3.58MG093	3.58	30	30	1.8	5.5
	CST3.58MGW093	3.58	On-chip	On-chip	1.8	5.5
	CSA4.19MG	4.19	30	30	2.0	5.5
	CST4.19MGW	4.19	On-chip	On-chip	2.0	5.5
	CSA4.19MG093	4.19	30	30	1.8	5.5
	CST4.19MGW093	4.19	On-chip	On-chip	1.8	5.5
	CSA5.00MG	5.00	30	30	2.0	5.5
	CST5.00MGW	5.00	On-chip	On-chip	2.0	5.5
	CSA5.00MG093	5.00	30	30	1.8	5.5
	CST5.00MGW093	5.00	On-chip	On-chip	1.8	5.5
	CSA8.00MTZ	8.00	30	30	4.0	5.5
	CST8.00MTW	8.00	On-chip	On-chip	4.0	5.5
	CSA8.00MTZ093	8.00	30	30	4.0	5.5
	CST8.00MTW093	8.00	On-chip	On-chip	4.0	5.5
	TDK	CCR3.58MC3	3.58	On-chip	On-chip	1.8
CCR4.19MC3		4.19	On-chip	On-chip	1.8	5.5
CCR5.0MC3		5.00	On-chip	On-chip	1.8	5.5
CCR8.0MC5		8.00	On-chip	On-chip	4.0	5.5
CCR8.38MC5		8.38	On-chip	On-chip	4.0	5.5

**Caution** The oscillator constant and oscillation voltage range indicate conditions of stable oscillation. Oscillation frequency precision is not guaranteed. For applications requiring oscillation frequency precision, the oscillation frequency must be adjusted on the implementation circuit. For details please contact directly the manufacturer of the resonator you will use.

DC Characteristics (T<sub>A</sub> = -40 to +85°C, V<sub>DD</sub> = 1.8 to 5.5 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Output current, high	I <sub>OH</sub>	Per pin				-1	mA
		All pins				-15	mA
Output current, low	I <sub>OL</sub>	Per pin for P00 to P03, P20 to P25, P34 to P36, P40 to P47, P64 to P67, P70 to P75				10	mA
		Per pin for P30 to P33, P50 to P57				15	mA
		Total for P00 to P03, P40 to P47, P64 to P67, P70 to P75				20	mA
		Total for P20 to P25				10	mA
		Total for P30 to P36				70	mA
		Total for P50 to P57				70	mA
Input voltage, high	V <sub>IH1</sub>	P10 to P17, P21, P24, P35, P40 to P47, P50 to P57, P64 to P67, P74, P75	V <sub>DD</sub> = 2.7 to 5.5 V	0.7 V <sub>DD</sub>		V <sub>DD</sub>	V
				0.8 V <sub>DD</sub>		V <sub>DD</sub>	V
	V <sub>IH2</sub>	P00 to P03, P20, P22, P23, P25, P34, P36, P70 to P73, RESET	V <sub>DD</sub> = 2.7 to 5.5 V	0.8 V <sub>DD</sub>		V <sub>DD</sub>	V
				0.85 V <sub>DD</sub>		V <sub>DD</sub>	V
	V <sub>IH3</sub>	P30 to P33 (N-ch open-drain)	V <sub>DD</sub> = 2.7 to 5.5 V	0.7 V <sub>DD</sub>		5.5	V
				0.8 V <sub>DD</sub>		5.5	V
	V <sub>IH4</sub>	X1, X2	V <sub>DD</sub> = 2.7 to 5.5 V	V <sub>DD</sub> -0.5		V <sub>DD</sub>	V
				V <sub>DD</sub> -0.2		V <sub>DD</sub>	V
	V <sub>IH5</sub>	XT1, XT2	V <sub>DD</sub> = 4.0 to 5.5 V	0.8 V <sub>DD</sub>		V <sub>DD</sub>	V
				0.9 V <sub>DD</sub>		V <sub>DD</sub>	V
Input voltage, low	V <sub>IL1</sub>	P10 to P17, P21, P24, P35, P40 to P47, P50 to P57, P64 to P67, P74, P75	V <sub>DD</sub> = 2.7 to 5.5 V	0		0.3 V <sub>DD</sub>	V
				0		0.2 V <sub>DD</sub>	V
	V <sub>IL2</sub>	P00 to P03, P20, P22, P23, P25, P34, P36, P70 to P73, RESET	V <sub>DD</sub> = 2.7 to 5.5 V	0		0.2 V <sub>DD</sub>	V
				0		0.15 V <sub>DD</sub>	V
				0		0.1 V <sub>DD</sub>	V
	V <sub>IL3</sub>	P30 to P33	4.0 V ≤ V <sub>DD</sub> ≤ 5.5 V	0		0.3 V <sub>DD</sub>	V
			2.7 V ≤ V <sub>DD</sub> < 4.0 V	0		0.2 V <sub>DD</sub>	V
			1.8 V ≤ V <sub>DD</sub> < 2.7	0		0.1 V <sub>DD</sub>	V
	V <sub>IL4</sub>	X1, X2	V <sub>DD</sub> = 2.7 to 5.5 V	0		0.4	V
				0		0.2	V
V <sub>IL5</sub>	XT1, XT2	V <sub>DD</sub> = 4.0 to 5.5 V	0		0.2 V <sub>DD</sub>	V	
			0		0.1 V <sub>DD</sub>	V	
Output voltage, high	V <sub>OH1</sub>	V <sub>DD</sub> = 4.0 to 5.5 V, I <sub>OH</sub> = -1 mA		V <sub>DD</sub> -1.0		V <sub>DD</sub>	V
		I <sub>OH</sub> = -100 μA		V <sub>DD</sub> -0.5		V <sub>DD</sub>	V
Output voltage, low	V <sub>OL1</sub>	P30 to P33	V <sub>DD</sub> = 4.0 to 5.5 V, I <sub>OL</sub> = 15 mA			2.0	V
		P50 to P57			0.4	2.0	V
		P00 to P03, P20 to P25, P34 to P36, P40 to P47, P64 to P67, P70 to P75				0.4	V
	V <sub>OL2</sub>	I <sub>OL</sub> = 400 μA				0.5	V

**Remark** Unless specified otherwise, the characteristics of alternate-function pins are the same as those of port pins.



DC Characteristics (T<sub>A</sub> = -40 to +85°C, V<sub>DD</sub> = 1.8 to 5.5 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Input leakage current, high	I <sub>LIH1</sub>	V <sub>IN</sub> = V <sub>DD</sub>	P00 to P03, P10 to P17, P20 to P25, P34 to P36, P40 to P47, P50 to P57, P64 to P67, P70 to P75, $\overline{\text{RESET}}$			3	μA
	I <sub>LIH2</sub>		X1, X2, XT1, XT2			20	μA
	I <sub>LIH3</sub>	V <sub>IN</sub> = 5.5 V	P30 to P33			3	μA
Input leakage current, low	I <sub>LIL1</sub>	V <sub>IN</sub> = 0 V	P00 to P03, P10 to P17, P20 to P25, P34 to P36, P40 to P47, P50 to P57, P64 to P67, P70 to P75, $\overline{\text{RESET}}$			-3	μA
	I <sub>LIL2</sub>		X1, X2, XT1, XT2			-20	μA
	I <sub>LIL3</sub>		P30 to P33			-3	μA
Output leakage current, low	I <sub>LOH</sub>	V <sub>OUT</sub> = V <sub>DD</sub>				3	μA
Output leakage current, low	I <sub>LOL</sub>	V <sub>OUT</sub> = 0 V				-3	μA
Software pull-up resistor	R	V <sub>IN</sub> = 0 V, P00 to P03, P20 to P25, P34 to P36, P40 to P47, P50 to P57, P64 to P67, P70 to P75		15	30	90	kΩ

**Remark** Unless specified otherwise, the characteristics of alternate-function pins are the same as those of port pins .

DC Characteristics (T<sub>A</sub> = -40 to +85°C, V<sub>DD</sub> = 1.8 to 5.5 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit	
Supply current <sup>Note 1</sup>	I <sub>DD1</sub>	8.38-MHz crystal oscillation operating mode	V <sub>DD</sub> = 5.0 V ± 10 % <sup>Note 2</sup>	A/D converter stopped		10.5	21	mA
				A/D converter operating		11.5	23	mA
		5.00-MHz crystal oscillation operation mode	V <sub>DD</sub> = 3.0 V ± 10 % <sup>Note 2</sup>	A/D converter stopped		4.5	9	mA
				A/D converter operating		5.5	11	mA
		V <sub>DD</sub> = 2.0 V ± 10 % <sup>Note 3</sup>	A/D converter stopped		1	2	mA	
			A/D converter operating		2	6	mA	
	I <sub>DD2</sub>	8.38-MHz crystal oscillation HALT mode	V <sub>DD</sub> = 5.0 V ± 10 % <sup>Note 2</sup>	Peripheral functions stopped		1.2	2.4	mA
				Peripheral functions operating			5	mA
		5.00-MHz crystal oscillation HALT mode	V <sub>DD</sub> = 3.0 V ± 10 % <sup>Note 2</sup>	Peripheral functions stopped		0.4	0.8	mA
				Peripheral functions operating			1.7	mA
		V <sub>DD</sub> = 2.0 V ± 10 % <sup>Note 3</sup>	Peripheral functions stopped		0.2	0.4	mA	
			Peripheral functions operating			1.1	mA	
	I <sub>DD3</sub>	32.768-kHz crystal oscillation operating mode <sup>Note 4</sup>	V <sub>DD</sub> = 5.0 V ± 10 % <sup>Note 2</sup>	V <sub>DD</sub> = 5.0 V ± 10 % <sup>Note 2</sup>		115	230	μA
				V <sub>DD</sub> = 3.0 V ± 10 % <sup>Note 2</sup>		95	190	μA
				V <sub>DD</sub> = 2.0 V ± 10 % <sup>Note 3</sup>		75	150	μA
I <sub>DD4</sub>	32.768-kHz crystal oscillation HALT mode <sup>Note 4</sup>	V <sub>DD</sub> = 5.0 V ± 10 % <sup>Note 2</sup>	V <sub>DD</sub> = 5.0 V ± 10 % <sup>Note 2</sup>		30	60	μA	
			V <sub>DD</sub> = 3.0 V ± 10 % <sup>Note 2</sup>		6	18	μA	
			V <sub>DD</sub> = 2.0 V ± 10 % <sup>Note 3</sup>		2	10	μA	
I <sub>DD5</sub>	XT1 = 0 V, STOP mode When feed-back resistor not used	V <sub>DD</sub> = 5.0 V ± 10 % <sup>Note 2</sup>	V <sub>DD</sub> = 5.0 V ± 10 % <sup>Note 2</sup>		0.1	30	μA	
			V <sub>DD</sub> = 3.0 V ± 10 % <sup>Note 2</sup>		0.05	10	μA	
			V <sub>DD</sub> = 2.0 V ± 10 % <sup>Note 3</sup>		0.05	10	μA	

- Notes**
1. Refers to the total current flowing through the internal power supply (V<sub>DD0</sub> and V<sub>DD1</sub>). Includes peripheral operating current (however, current flowing through the pull-up resistors of ports and the AV<sub>REF</sub> pin is not included).
  2. When the processor clock control register (PCC) is set to 00H.
  3. When PCC is set to 02H.
  4. When the main system clock is stopped.

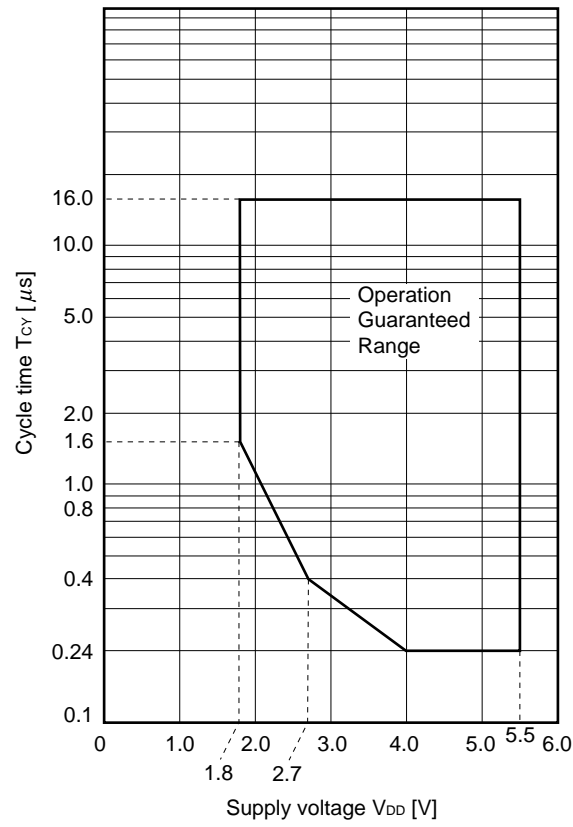
AC Characteristics

(1) Basic operation (T<sub>A</sub> = -40 to +85°C, V<sub>DD</sub> = 1.8 to 5.5 V)

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit	
Cycle time (Min. instruction execution time)	T <sub>CY</sub>	Operating on main system clock	4.0 V ≤ V <sub>DD</sub> ≤ 5.5 V	0.24		16	μs
			2.7 V ≤ V <sub>DD</sub> < 4.0 V	0.4		16	μs
				1.6		16	μs
		Operating on subsystem clock	103.9 <sup>Note 1</sup>	122	125	μs	
TI00, TI01 input high-/low-level width	t <sub>TIH0</sub> , t <sub>TIL0</sub>	4.0 V ≤ V <sub>DD</sub> ≤ 5.5 V	2f <sub>sam</sub> + 0.1 <sup>Note2</sup>			μs	
		2.7 V ≤ V <sub>DD</sub> < 4.0 V	2f <sub>sam</sub> + 0.2 <sup>Note2</sup>			μs	
			2f <sub>sam</sub> + 0.5 <sup>Note2</sup>			μs	
TI50, TI51 input frequency	f <sub>TI5</sub>	V <sub>DD</sub> = 2.7 to 5.5 V	0		4	MHz	
			0		275	kHz	
TI50, TI51 input high-/low-level width	t <sub>TIH5</sub> , t <sub>TIL5</sub>	V <sub>DD</sub> = 2.7 to 5.5 V	100			ns	
			1.8			μs	
Interrupt request input high-/low -level width	t <sub>INTH</sub> , t <sub>INTL</sub>	INTP0 to INTP3, P40 to P47	V <sub>DD</sub> = 2.7 to 5.5 V	1			μs
				2			μs
RESET low-level width	t <sub>RSL</sub>	V <sub>DD</sub> = 2.7 to 5.5 V		10			μs
				20			μs

- Notes**
- Value when using an external clock. When using a crystal resonator, the value becomes 114 μs (MIN.).
  - Selection of f<sub>sam</sub> = f<sub>x</sub>, f<sub>x</sub>/4, f<sub>x</sub>/64 is possible using bits 0 and 1 (PRM00, PRM01) of prescaler mode register 0 (PRM0). However, if the TI00 valid edge is selected as the count clock, the value becomes f<sub>sam</sub> = f<sub>x</sub>/8.

T<sub>CY</sub> vs V<sub>DD</sub> (main system clock)



(2) Read/write operation (T<sub>A</sub> = -40 to +85°C, V<sub>DD</sub> = 4.0 to 5.5 V) (1/3)

Parameter	Symbol	Test Conditions	MIN.	MAX.	Unit
ASTB high-level width	t <sub>ASTH</sub>		0.3t <sub>cy</sub>		ns
Address setup time	t <sub>ADS</sub>		20		ns
Address hold time	t <sub>ADH</sub>		6		ns
Data input time from address	t <sub>ADD1</sub>			(2 + 2n)t <sub>cy</sub> - 54	ns
	t <sub>ADD2</sub>			(3 + 2n)t <sub>cy</sub> - 60	ns
Address output time from $\overline{RD}\downarrow$	t <sub>RDAD</sub>		0	100	ns
Data input time from $\overline{RD}\downarrow$	t <sub>RDD1</sub>			(2 + 2n)t <sub>cy</sub> - 87	ns
	t <sub>RDD2</sub>			(3 + 2n)t <sub>cy</sub> - 93	ns
Read data hold time	t <sub>RDH</sub>		0		ns
$\overline{RD}$ low-level width	t <sub>RDL1</sub>		(1.5 + 2n)t <sub>cy</sub> - 33		ns
	t <sub>RDL2</sub>		(2.5 + 2n)t <sub>cy</sub> - 33		ns
$\overline{WAIT}\downarrow$ input time from $\overline{RD}\downarrow$	t <sub>RDWT1</sub>			t <sub>cy</sub> - 43	ns
	t <sub>RDWT2</sub>			t <sub>cy</sub> - 43	ns
$\overline{WAIT}\downarrow$ input time from $\overline{WR}\downarrow$	t <sub>WRWT</sub>			t <sub>cy</sub> - 25	ns
$\overline{WAIT}$ low-level width	t <sub>WTL</sub>		(0.5 + n)t <sub>cy</sub> + 10	(2 + 2n)t <sub>cy</sub>	ns
Write data setup time	t <sub>WDS</sub>		60		ns
Write data hold time	t <sub>WDH</sub>		6		ns
$\overline{WR}$ low-level width	t <sub>WRL1</sub>		(1.5 + 2n)t <sub>cy</sub> - 15		ns
$\overline{RD}\downarrow$ delay time from $\overline{ASTB}\downarrow$	t <sub>ASTRD</sub>		6		ns
$\overline{WR}\downarrow$ delay time from $\overline{ASTB}\downarrow$	t <sub>ASTWR</sub>		2t <sub>cy</sub> - 15		ns
ASTB $\uparrow$ delay time from $\overline{RD}\uparrow$ in external fetch	t <sub>RDAST</sub>		0.8t <sub>cy</sub> - 15	1.2t <sub>cy</sub>	ns
Address hold time from $\overline{RD}\uparrow$ in external fetch	t <sub>RDADH</sub>		0.8t <sub>cy</sub> - 15	1.2t <sub>cy</sub> + 30	ns
Write data output time from $\overline{RD}\uparrow$	t <sub>RDWD</sub>		40		ns
Write data output time from $\overline{WR}\downarrow$	t <sub>WRWD</sub>		10	60	ns
Address hold time from $\overline{WR}\uparrow$	t <sub>WRADH</sub>		0.8t <sub>cy</sub> - 15	1.2t <sub>cy</sub> + 30	ns
$\overline{RD}\uparrow$ delay time from $\overline{WAIT}\uparrow$	t <sub>WTRD</sub>		0.8t <sub>cy</sub>	2.5t <sub>cy</sub> + 25	ns
$\overline{WR}\uparrow$ delay time from $\overline{WAIT}\uparrow$	t <sub>WTWR</sub>		0.8t <sub>cy</sub>	2.5t <sub>cy</sub> + 25	ns

**Remarks** 1. t<sub>cy</sub> = T<sub>cy</sub>/4

2. n indicates the number of waits.

3. C<sub>L</sub> = 100 pF (C<sub>L</sub> is the load capacitance of the AD0 to AD7, A8 to A15,  $\overline{RD}$ ,  $\overline{WR}$ ,  $\overline{WAIT}$ , and ASTB pins.)

(2) Read/write operation (T<sub>A</sub> = -40 to +85°C, V<sub>DD</sub> = 2.7 to 4.0 V) (2/3)

Parameter	Symbol	Test Conditions	MIN.	MAX.	Unit
ASTB high-level width	t <sub>ASTH</sub>		0.3t <sub>cy</sub>		ns
Address setup time	t <sub>ADS</sub>		30		ns
Address hold time	t <sub>ADH</sub>		10		ns
Data input time from address	t <sub>ADD1</sub>			(2 + 2n)t <sub>cy</sub> - 108	ns
	t <sub>ADD2</sub>			(3 + 2n)t <sub>cy</sub> - 120	ns
Address output time from $\overline{RD}\downarrow$	t <sub>RDAD</sub>		0	200	ns
Data input time from $\overline{RD}\downarrow$	t <sub>RDD1</sub>			(2 + 2n)t <sub>cy</sub> - 148	ns
	t <sub>RDD2</sub>			(3 + 2n)t <sub>cy</sub> - 162	ns
Read data hold time	t <sub>RDH</sub>		0		ns
$\overline{RD}$ low-level width	t <sub>RDL1</sub>		(1.5 + 2n)t <sub>cy</sub> - 40		ns
	t <sub>RDL2</sub>		(2.5 + 2n)t <sub>cy</sub> - 40		ns
$\overline{WAIT}\downarrow$ input time from $\overline{RD}\downarrow$	t <sub>RDWT1</sub>			t <sub>cy</sub> - 75	ns
	t <sub>RDWT2</sub>			t <sub>cy</sub> - 60	ns
$\overline{WAIT}\downarrow$ input time from $\overline{WR}\downarrow$	t <sub>WRWT</sub>			t <sub>cy</sub> - 50	ns
$\overline{WAIT}$ low-level width	t <sub>WTL</sub>		(0.5 + 2n)t <sub>cy</sub> + 10	(2 + 2n)t <sub>cy</sub>	ns
Write data setup time	t <sub>WDS</sub>		60		ns
Write data hold time	t <sub>WDH</sub>		10		ns
$\overline{WR}$ low-level width	t <sub>WRL1</sub>		(1.5 + 2n)t <sub>cy</sub> - 30		ns
$\overline{RD}\downarrow$ delay time from $\overline{ASTB}\downarrow$	t <sub>ASTRD</sub>		10		ns
$\overline{WR}\downarrow$ delay time from $\overline{ASTB}\downarrow$	t <sub>ASTWR</sub>		2t <sub>cy</sub> - 30		ns
ASTB $\uparrow$ delay time from $\overline{RD}\uparrow$ in external fetch	t <sub>RDAST</sub>		0.8t <sub>cy</sub> - 30	1.2t <sub>cy</sub>	ns
Address hold time from $\overline{RD}\uparrow$ in external fetch	t <sub>RDADH</sub>		0.8t <sub>cy</sub> - 30	1.2t <sub>cy</sub> + 60	ns
Write data output time from $\overline{RD}\uparrow$	t <sub>RDWD</sub>		40		ns
Write data output time from $\overline{WR}\downarrow$	t <sub>WRWD</sub>		20	120	ns
Address hold time from $\overline{WR}\uparrow$	t <sub>WRADH</sub>		0.8t <sub>cy</sub> - 30	1.2t <sub>cy</sub> + 60	ns
$\overline{RD}\uparrow$ delay time from $\overline{WAIT}\uparrow$	t <sub>WTRD</sub>		0.5t <sub>cy</sub>	2.5t <sub>cy</sub> + 50	ns
$\overline{WR}\uparrow$ delay time from $\overline{WAIT}\uparrow$	t <sub>WTWR</sub>		0.5t <sub>cy</sub>	2.5t <sub>cy</sub> + 50	ns

- Remarks**
1. t<sub>cy</sub> = T<sub>cy</sub>/4
  2. n indicates the number of waits.
  3. C<sub>L</sub> = 100 pF (C<sub>L</sub> is the load capacitance of the AD0 to AD7, A8 to A15,  $\overline{RD}$ ,  $\overline{WR}$ ,  $\overline{WAIT}$ , and ASTB pins.)

(2) Read/write operation (T<sub>A</sub> = -40 to +85°C, V<sub>DD</sub> = 1.8 to 2.7 V) (3/3)

Parameter	Symbol	Test Conditions	MIN.	MAX.	Unit
ASTB high-level width	t <sub>ASTH</sub>		0.3t <sub>cy</sub>		ns
Address setup time	t <sub>ADS</sub>		120		ns
Address hold time	t <sub>ADH</sub>		20		ns
Data input time from address	t <sub>ADD1</sub>			(2 + 2n)t <sub>cy</sub> - 233	ns
	t <sub>ADD2</sub>			(3 + 2n)t <sub>cy</sub> - 240	ns
Address output time from $\overline{RD}\downarrow$	t <sub>RDAD</sub>		0	400	ns
Data input time from $\overline{RD}\downarrow$	t <sub>RDD1</sub>			(2 + 2n)t <sub>cy</sub> - 325	ns
	t <sub>RDD2</sub>			(3 + 2n)t <sub>cy</sub> - 332	ns
Read data hold time	t <sub>RDH</sub>		0		ns
$\overline{RD}$ low-level width	t <sub>RDL1</sub>		(1.5 + 2n)t <sub>cy</sub> - 92		ns
	t <sub>RDL2</sub>		(2.5 + 2n)t <sub>cy</sub> - 92		ns
$\overline{WAIT}\downarrow$ input time from $\overline{RD}\downarrow$	t <sub>RDWT1</sub>			t <sub>cy</sub> - 350	ns
	t <sub>RDWT2</sub>			t <sub>cy</sub> - 132	ns
$\overline{WAIT}\downarrow$ input time from $\overline{WR}\downarrow$	t <sub>WRWT</sub>			t <sub>cy</sub> - 100	ns
$\overline{WAIT}$ low-level width	t <sub>WTL</sub>		(0.5 + 2n)t <sub>cy</sub> + 10	(2 + 2n)t <sub>cy</sub>	ns
Write data setup time	t <sub>WDS</sub>		60		ns
Write data hold time	t <sub>WDH</sub>		20		ns
$\overline{WR}$ low-level width	t <sub>WRL1</sub>		(1.5 + 2n)t <sub>cy</sub> - 60		ns
$\overline{RD}\downarrow$ delay time from $\overline{ASTB}\downarrow$	t <sub>ASTRD</sub>		20		ns
$\overline{WR}\downarrow$ delay time from $\overline{ASTB}\downarrow$	t <sub>ASTWR</sub>		2t <sub>cy</sub> - 60		ns
ASTB $\uparrow$ delay time from $\overline{RD}\uparrow$ at external fetch	t <sub>RDAST</sub>		0.8t <sub>cy</sub> - 60	1.2t <sub>cy</sub>	ns
Address hold time from $\overline{RD}\uparrow$ at external fetch	t <sub>RDADH</sub>		0.8t <sub>cy</sub> - 60	1.2t <sub>cy</sub> + 120	ns
Write data output time from $\overline{RD}\uparrow$	t <sub>RDWD</sub>		40		ns
Write data output time from $\overline{WR}\downarrow$	t <sub>WRWD</sub>		40	240	ns
Address hold time from $\overline{WR}\uparrow$	t <sub>WRADH</sub>		0.8t <sub>cy</sub> - 60	1.2t <sub>cy</sub> + 120	ns
$\overline{RD}\uparrow$ delay time from $\overline{WAIT}\uparrow$	t <sub>WTRD</sub>		0.5t <sub>cy</sub>	2.5t <sub>cy</sub> + 100	ns
$\overline{WR}\uparrow$ delay time from $\overline{WAIT}\uparrow$	t <sub>WTWR</sub>		0.5t <sub>cy</sub>	2.5t <sub>cy</sub> + 100	ns

**Remarks** 1. t<sub>cy</sub> = T<sub>cy</sub>/4

2. n indicates the number of waits.

3. C<sub>L</sub> = 100 pF (C<sub>L</sub> is the load capacitance of the AD0 to AD7, A8 to A15,  $\overline{RD}$ ,  $\overline{WR}$ ,  $\overline{WAIT}$ , and ASTB pins.)

(3) Serial interface (T<sub>A</sub> = -40 to +85°C, V<sub>DD</sub> = 1.8 to 5.5 V)

(a) 3-wire serial I/O mode ( $\overline{\text{SCK30}}$  and  $\overline{\text{SCK31}}$ ... internal clock output)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
$\overline{\text{SCK30}}$ , $\overline{\text{SCK31}}$ cycle time	t <sub>KCY1</sub>	4.0 V ≤ V <sub>DD</sub> ≤ 5.5 V	954			ns
		2.7 V ≤ V <sub>DD</sub> < 4.0 V	1600			ns
			3200			ns
$\overline{\text{SCK30}}$ , $\overline{\text{SCK31}}$ high-/low-level width	t <sub>KH1</sub>	V <sub>DD</sub> = 4.0 to 5.5 V	t <sub>KCY1</sub> /2-50			ns
	t <sub>KL1</sub>		t <sub>KCY1</sub> /2-100			ns
SI30, SI31 setup time (to $\overline{\text{SCK30}}$ , $\overline{\text{SCK31}}$ ↑)	t <sub>SIK1</sub>	4.0 V ≤ V <sub>DD</sub> ≤ 5.5 V	100			ns
		2.7 V ≤ V <sub>DD</sub> < 4.0 V	150			ns
			300			ns
SI30, SI31 hold time (from $\overline{\text{SCK30}}$ , $\overline{\text{SCK31}}$ ↑)	t <sub>SIH1</sub>		400			ns
SO30, SO31 output delay time from $\overline{\text{SCK30}}$ , $\overline{\text{SCK31}}$ ↓	t <sub>KSO1</sub>	C = 100 pF <sup>Note</sup>			300	ns

**Note** C is the load capacitance of the  $\overline{\text{SCK30}}$ ,  $\overline{\text{SCK31}}$ , SO30, and SO31 output lines.

(b) 3-wire serial I/O mode ( $\overline{\text{SCK30}}$ ,  $\overline{\text{SCK31}}$ ... external clock input)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
$\overline{\text{SCK30}}$ , $\overline{\text{SCK31}}$ cycle time	t <sub>KCY2</sub>	4.0 V ≤ V <sub>DD</sub> ≤ 5.5 V	800			ns
		2.7 V ≤ V <sub>DD</sub> < 4.0 V	1600			ns
			3200			ns
$\overline{\text{SCK30}}$ , $\overline{\text{SCK31}}$ high-/low-level width	t <sub>KH2</sub>	4.0 V ≤ V <sub>DD</sub> ≤ 5.5 V	400			ns
	t <sub>KL2</sub>	2.7 V ≤ V <sub>DD</sub> < 4.0 V	800			ns
			1600			ns
SI30, SI31 setup time (to $\overline{\text{SCK30}}$ , $\overline{\text{SCK31}}$ ↑)	t <sub>SIK2</sub>		100			ns
SI30, SI31 hold time (from $\overline{\text{SCK30}}$ , $\overline{\text{SCK31}}$ ↑)	t <sub>SIH2</sub>		400			ns
SO30, SO31 output delay time from $\overline{\text{SCK30}}$ , $\overline{\text{SCK31}}$ ↓	t <sub>KSO2</sub>	C = 100 pF <sup>Note</sup>			300	ns

**Note** C is the load capacitance of the SO30 and SO31 output lines.



**(c) UART mode (Dedicated baud rate generator output)**

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Transfer rate		$4.0\text{ V} \leq V_{DD} \leq 5.5\text{ V}$			131031	bps
		$2.7\text{ V} \leq V_{DD} < 4.0\text{ V}$			78125	bps
					39063	bps

**(d) UART mode (External clock input)**

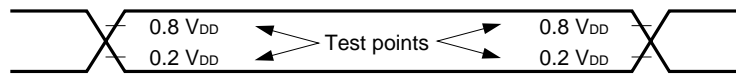
Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
ASCK0 cycle time	t <sub>KCY3</sub>	$4.0\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	800			ns
		$2.7\text{ V} \leq V_{DD} < 4.0\text{ V}$	1600			ns
			3200			ns
ASCK0 high-/low-level width	t <sub>KH3</sub> ,	$4.0\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	400			ns
	t <sub>KL3</sub>	$2.7\text{ V} \leq V_{DD} < 4.0\text{ V}$	800			ns
			1600			ns
Transfer rate		$4.0\text{ V} \leq V_{DD} \leq 5.5\text{ V}$			39063	bps
		$2.7\text{ V} \leq V_{DD} < 4.0\text{ V}$			19531	bps
					9766	bps

**(e) UART mode (Infrared data transfer mode)**

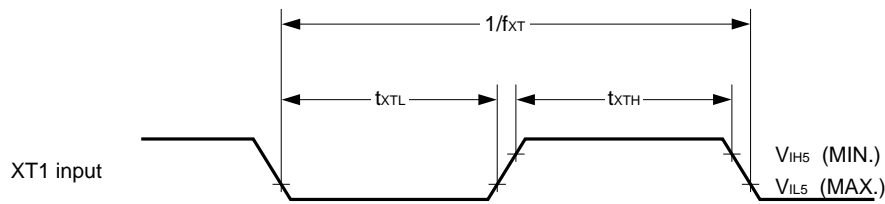
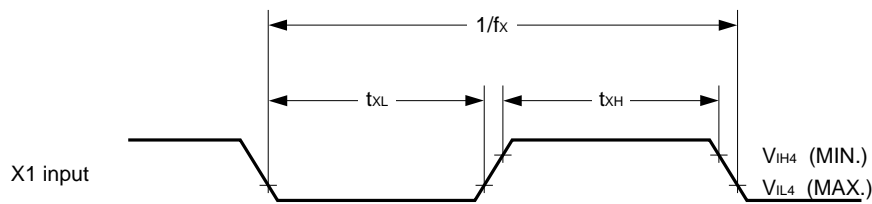
Parameter	Symbol	Conditions	MIN.	MAX.	Unit
Transfer rate		$V_{DD} = 4.0\text{ to }5.5\text{ V}$		131031	bps
Bit rate allowable error		$V_{DD} = 4.0\text{ to }5.5\text{ V}$		±0.87	%
Output pulse width		$V_{DD} = 4.0\text{ to }5.5\text{ V}$	1.2	0.24/fbr <sup>Note</sup>	μs
Input pulse width		$V_{DD} = 4.0\text{ to }5.5\text{ V}$	4/fx		μs

**Note** fbr: set baud rate

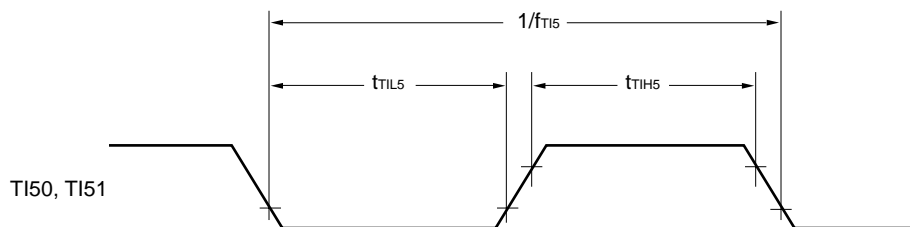
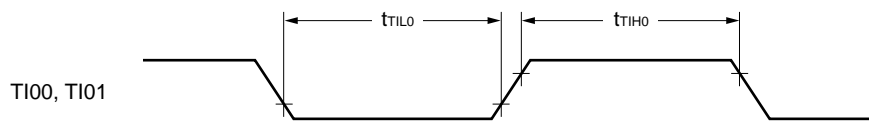
AC Timing Test Point (Excluding X1, XT1 Input)



Clock Timing

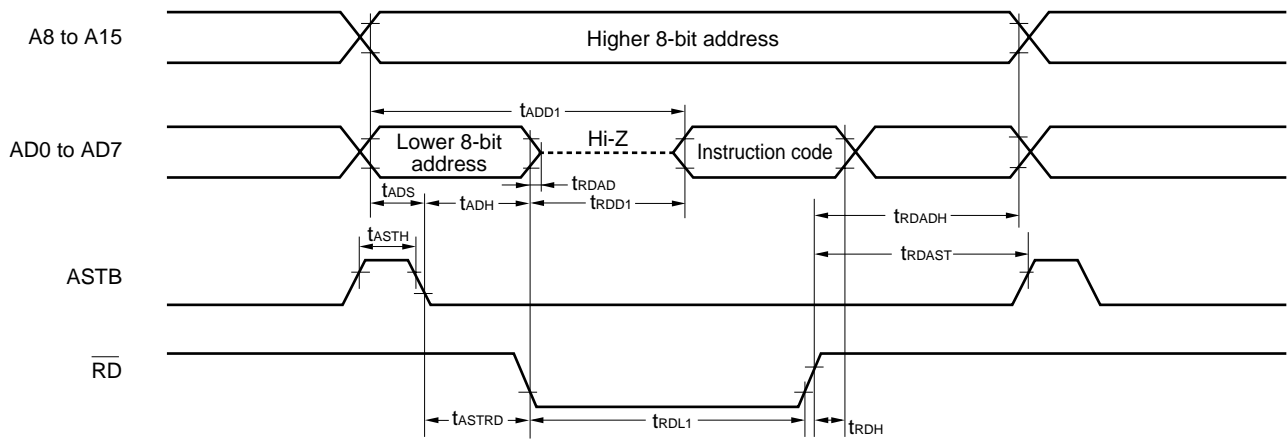


TI Timing

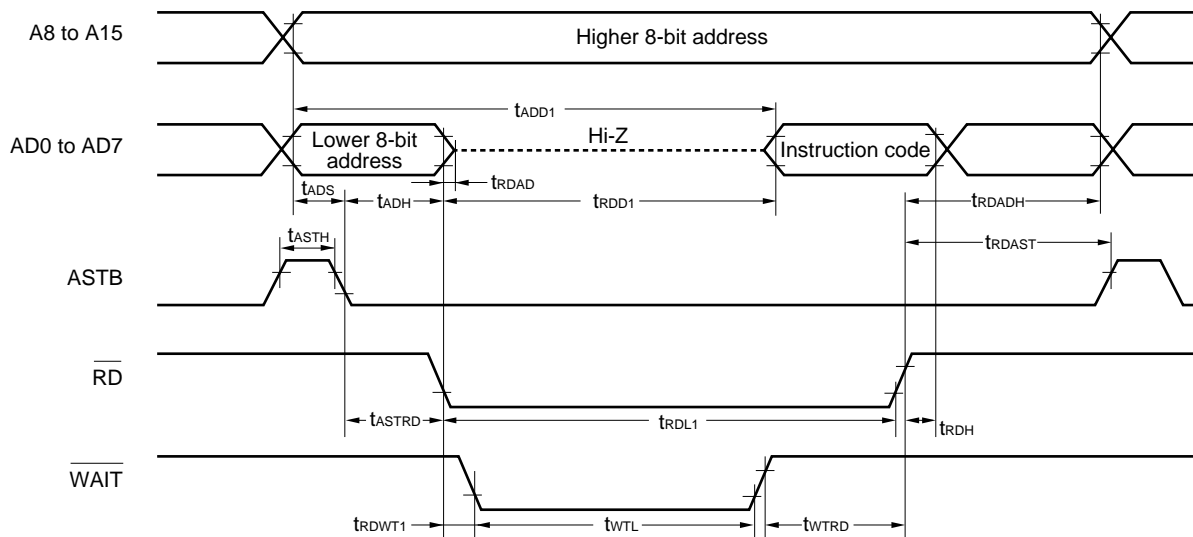


Read/Write Operation

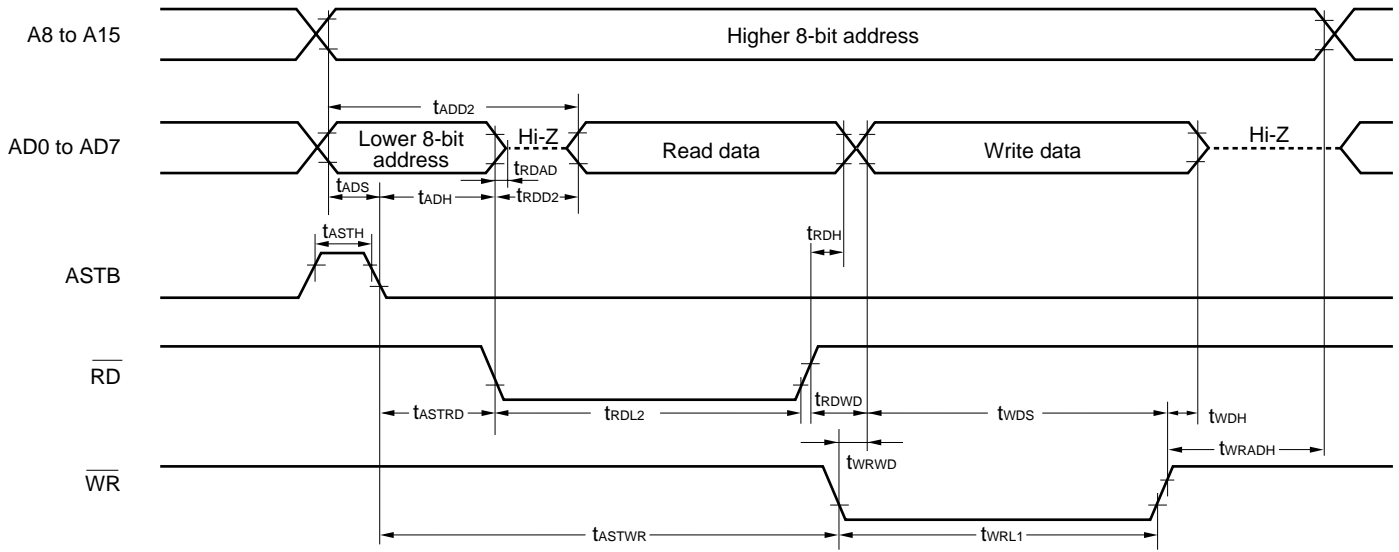
External Fetch (No Wait):



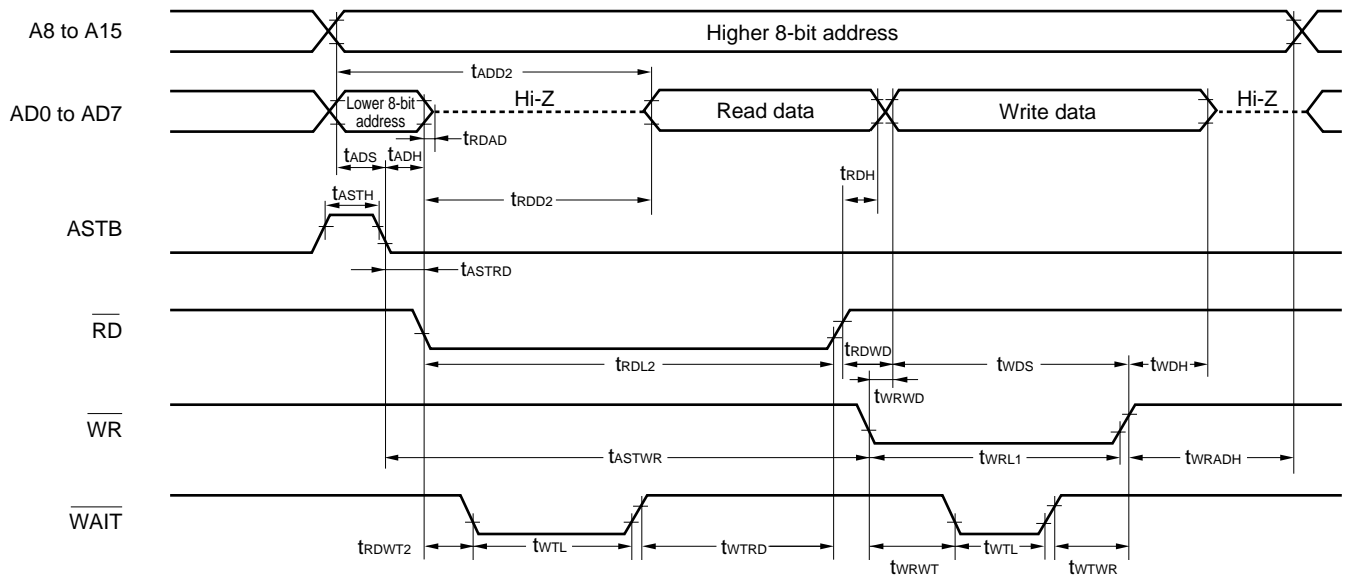
External Fetch (Wait Insertion):



**External Data Access (No Wait):**

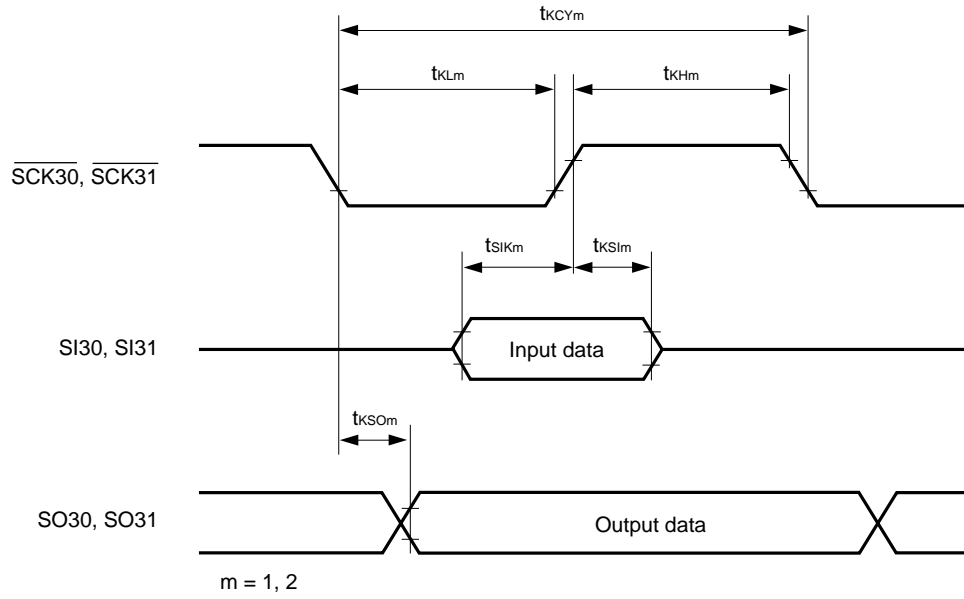


**External Data Access (Wait Insertion):**

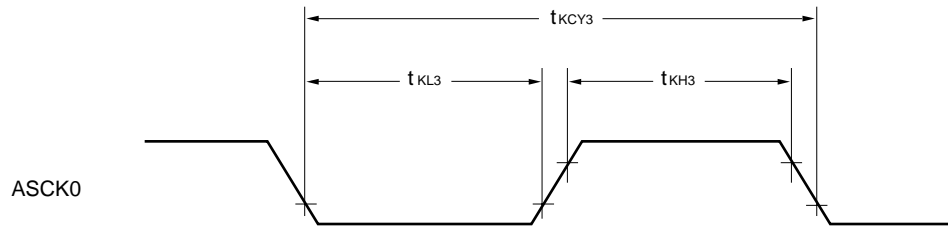


Serial Transfer Timing

3-Wire Serial I/O Mode:



UART Mode (External Clock Input):



**A/D Converter Characteristics (T<sub>A</sub> = -40 to +85°C, V<sub>DD</sub> = AV<sub>DD</sub> = AV<sub>REF</sub> = 1.8 to 5.5 V, AV<sub>SS</sub> = V<sub>SS</sub> = 0 V)**

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Resolution			10	10	10	bit
Overall error <sup>Note</sup>		4.0 V ≤ AV <sub>REF</sub> ≤ 5.5 V		±0.2	±0.4	%FSR
		2.7 V ≤ AV <sub>REF</sub> < 4.0 V		±0.3	±0.6	%FSR
		1.8 V ≤ AV <sub>REF</sub> < 2.7 V		±0.6	±1.2	%FSR
Conversion time	t <sub>CONV</sub>	4.0 V ≤ AV <sub>REF</sub> ≤ 5.5 V	14		96	μs
		2.7 V ≤ AV <sub>REF</sub> < 4.0 V	19		96	μs
		1.8 V ≤ AV <sub>REF</sub> < 2.7 V	28		96	μs
Zero-scale offset <sup>Note</sup>		4.0 V ≤ AV <sub>REF</sub> ≤ 5.5 V			±0.4	%FSR
		2.7 V ≤ AV <sub>REF</sub> < 4.0 V			±0.6	%FSR
		1.8 V ≤ AV <sub>REF</sub> < 2.7 V			±1.2	%FSR
Full-scale offset <sup>Note</sup>		4.0 V ≤ AV <sub>REF</sub> ≤ 5.5 V			±0.4	%FSR
		2.7 V ≤ AV <sub>REF</sub> < 4.0 V			±0.6	%FSR
		1.8 V ≤ AV <sub>REF</sub> < 2.7 V			±1.2	%FSR
Non-linearity error <sup>Note</sup>		4.0 V ≤ AV <sub>REF</sub> ≤ 5.5 V			±2.5	LSB
		2.7 V ≤ AV <sub>REF</sub> < 4.0 V			±4.5	LSB
		1.8 V ≤ AV <sub>REF</sub> < 2.7 V			±8.5	LSB
Differential non-linearity error		4.0 V ≤ AV <sub>REF</sub> ≤ 5.5 V			±1.5	LSB
		2.7 V ≤ AV <sub>REF</sub> < 4.0 V			±2.0	LSB
		1.8 V ≤ AV <sub>REF</sub> < 2.7 V			±3.5	LSB
Analog input voltage	V <sub>IAN</sub>		0		AV <sub>REF</sub>	V
Reference voltage	AV <sub>REF</sub>		1.8		AV <sub>DD</sub>	V
Resistance between AV <sub>REF</sub> and AV <sub>SS</sub>	R <sub>REF</sub>	A/D conversion is not performed	20	40		kΩ

**Note** Excluding quantization error (±1/2 LSB). Shown as a percentage of the full scale value.

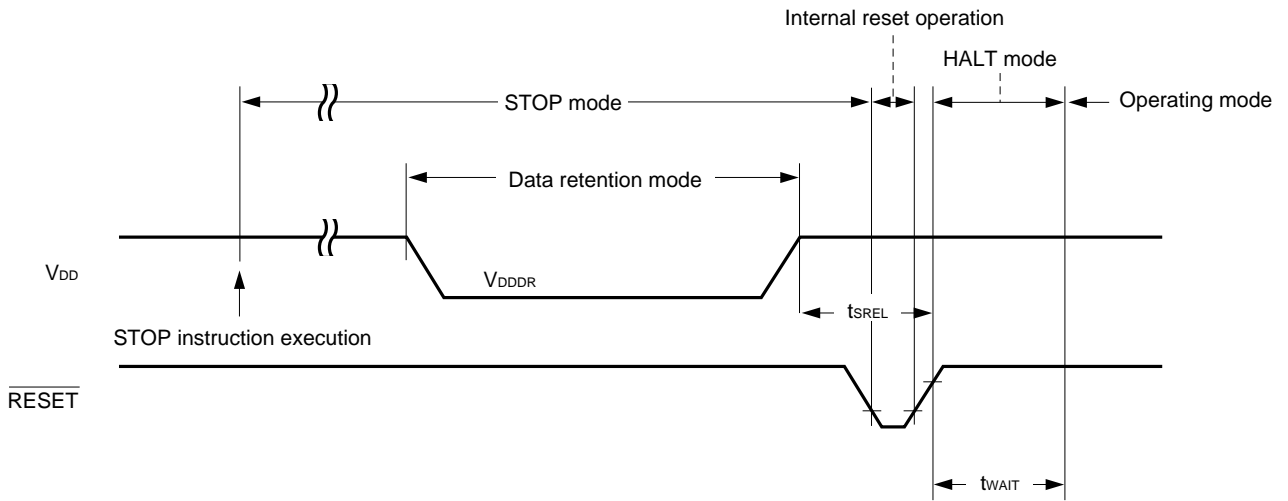
**Remark** When the μPD78F0034A is used as an 8-bit resolution A/D converter, the specifications are the same as for the μPD780024A Subseries A/D converter.

**Data Memory STOP Mode Low Supply Voltage Data Retention Characteristics (T<sub>A</sub> = -40 to +85°C)**

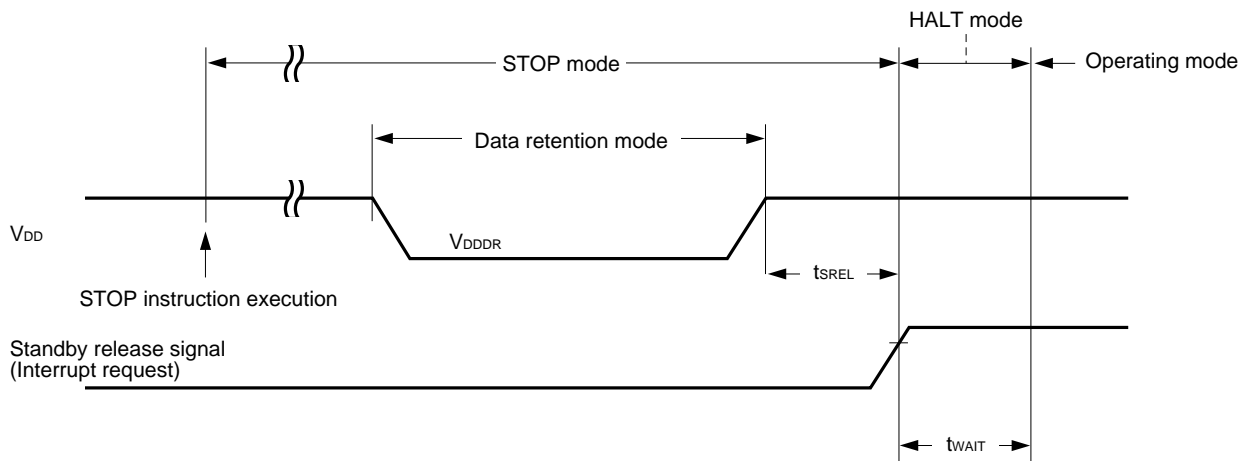
Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
Data retention supply voltage	V <sub>DDDR</sub>		1.6		5.5	V
Data retention supply current	I <sub>DDDR</sub>	V <sub>DDDR</sub> = 1.6 V Subsystem clock unassigned and feed-back resistor disconnected		0.1	30	μA
Release signal set time	t <sub>SREL</sub>		0			μs
Oscillation stabilization wait time	t <sub>WAIT</sub>	Release by RESET		2 <sup>17</sup> /f <sub>x</sub>		ms
		Release by interrupt request		<b>Note</b>		ms

**Note** Selection of 2<sup>12</sup>/f<sub>x</sub> and 2<sup>14</sup>/f<sub>x</sub> to 2<sup>17</sup>/f<sub>x</sub> is possible using bits 0 to 2 (OSTS0 to OSTS2) of the oscillation stabilization time select register (OSTS).

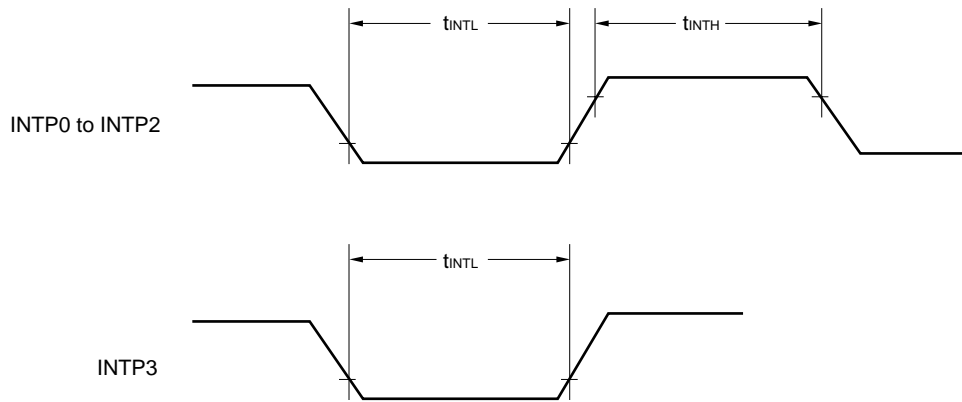
Data Retention Timing (STOP Mode Release by  $\overline{\text{RESET}}$ )



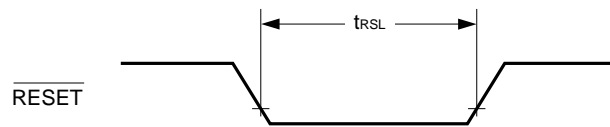
Data Retention Timing (Standby Release Signal: STOP Mode Release by Interrupt Request Signal)



Interrupt Request Input Timing



$\overline{\text{RESET}}$  Input Timing





Flash Memory Programming Characteristics ( $V_{DD} = 2.7$  to  $5.5$  V,  $V_{SS} = 0$  V,  $V_{PP} = 9.7$  to  $10.3$  V)

(1) Basic characteristics

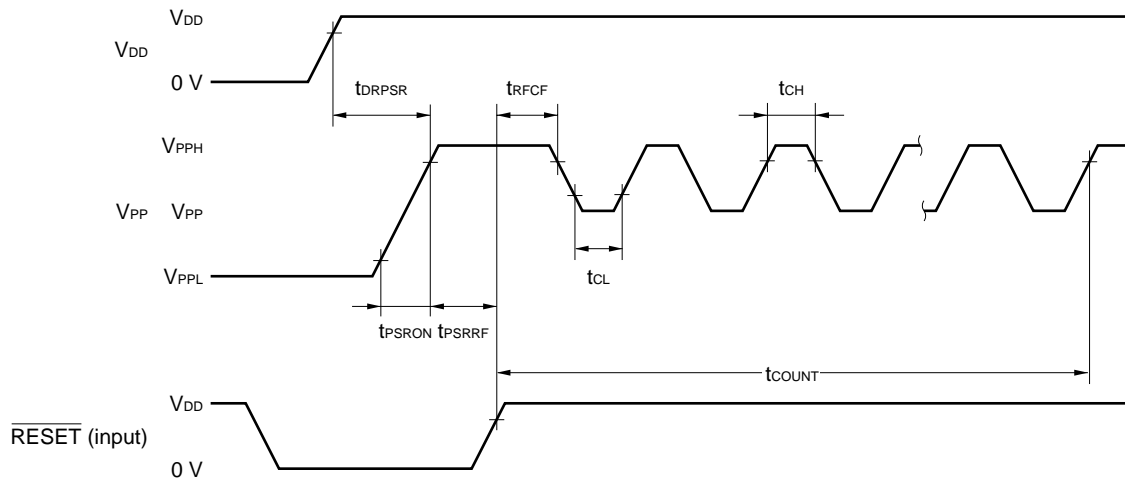
Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Operating frequency	$f_x$	$4.0 \leq V_{DD} \leq 5.5$ V	1.0		8.38	MHz
		$2.7 \leq V_{DD} < 4.0$ V	1.0		5.0	MHz
Supply voltage	$V_{DD}$	Operation voltage when writing	2.7		5.5	V
	$V_{PPL}$	Upon $V_{PP}$ low-level detection	0		$0.2 V_{DD}$	V
	$V_{PP}$	Upon $V_{PP}$ high-level detection	$0.8 V_{DD}$	$V_{DD}$	$1.2 V_{DD}$	V
	$V_{PPH}$	Upon $V_{PP}$ high-voltage detection	9.7 <sup>Note 1</sup>	10.0 <sup>Note 1</sup>	10.3 <sup>Note 1</sup>	V
$V_{DD}$ supply current	$I_{DD}$				10	mA
$V_{PP}$ supply current	$I_{PP}$	$V_{PP} = 10.0$ V		75	100	mA
Write time (per byte)	$T_{WRT}$		50		500	$\mu$ s
Number of rewrites	$C_{WRT}$				20 <sup>Note 2</sup>	Times
Erase time	$T_{ERASE}$		1		20	s
Programming temperature	$T_{PRG}$		+10		+40	$^{\circ}$ C

- Notes** 1. For the product grades "K, E, and P", 10.2 V (MIN.), 10.3 V (TYP.), and 10.4 V (MAX.), are applied.  
 2. For the product specification "K and E", the number is 1 (MAX.).

(2) Serial write operation characteristics

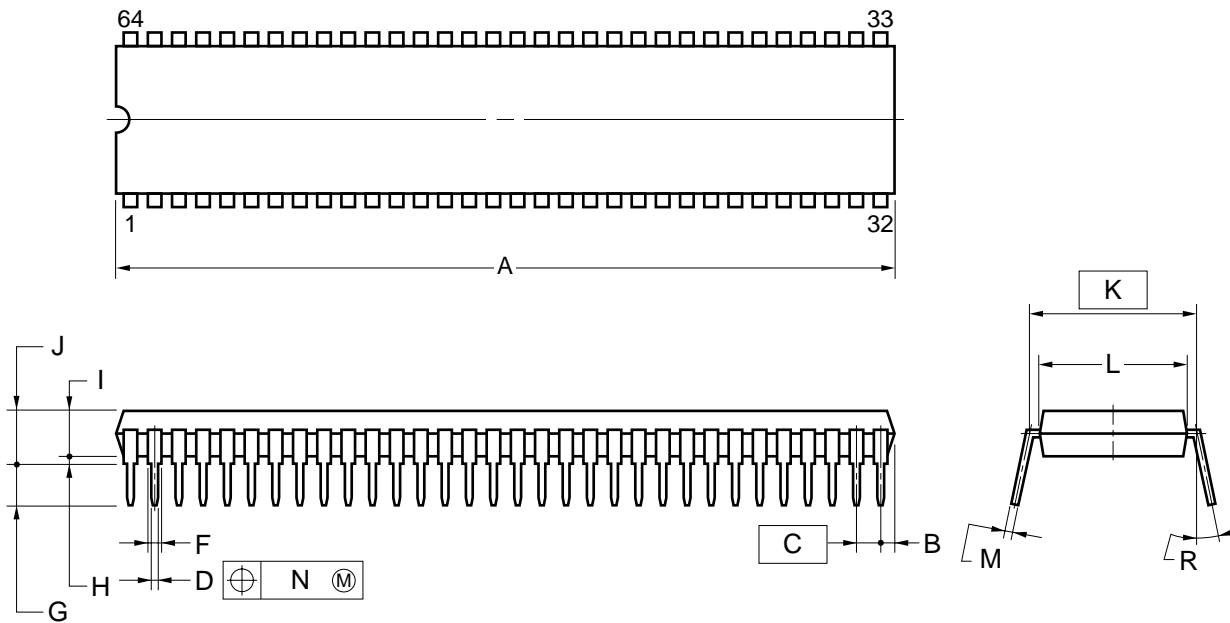
Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
$V_{PP}$ set time	$t_{PSRON}$	$V_{PP}$ high voltage	1.0			$\mu$ s
$V_{PP}\uparrow$ set time from $V_{DD}\uparrow$	$t_{DRPSR}$	$V_{PP}$ high voltage	1.0			$\mu$ s
$\overline{RESET}\uparrow$ set time from $V_{PP}\uparrow$	$t_{PSRRF}$	$V_{PP}$ high voltage	1.0			$\mu$ s
$V_{PP}$ count start time from $\overline{RESET}\uparrow$	$t_{RFCF}$		1.0			$\mu$ s
Count execution time	$t_{COUNT}$				2.0	ms
$V_{PP}$ counter high-level width	$t_{CH}$		8.0			$\mu$ s
$V_{PP}$ counter low-level width	$t_{CL}$		8.0			$\mu$ s
$V_{PP}$ counter noise elimination width	$t_{NFW}$			40		ns

Flash Memory Write Mode Set Timing



6. PACKAGE DRAWINGS

64 PIN PLASTIC SHRINK DIP (750 mil)



NOTES

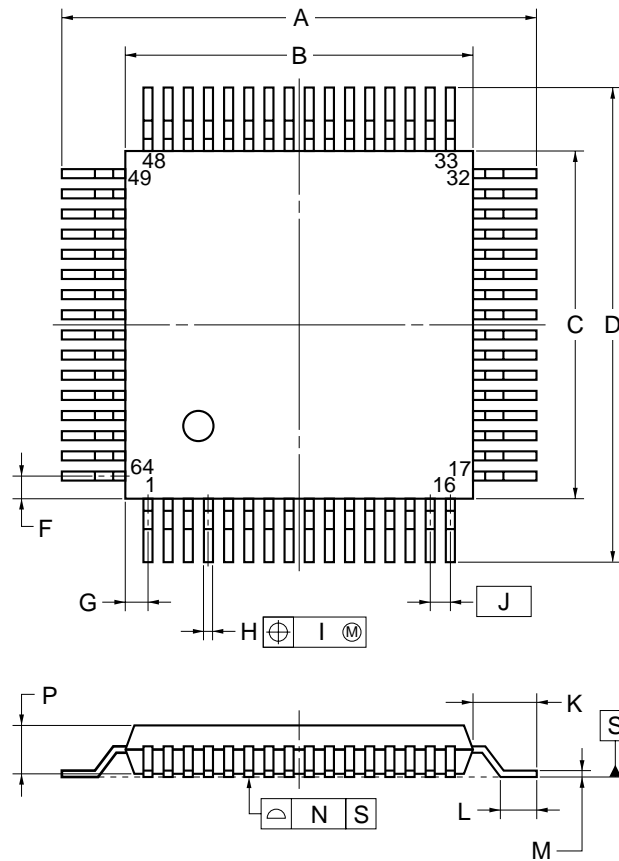
1. Controlling dimension— millimeter.
2. Each lead centerline is located within 0.17 mm (0.007 inch) of its true position (T.P.) at maximum material condition.
3. Item "K" to center of leads when formed parallel.

ITEM	MILLIMETERS	INCHES
A	58.0 <sup>+0.68</sup> <sub>-0.20</sub>	2.283 <sup>+0.028</sup> <sub>-0.008</sub>
B	1.78 MAX.	0.070 MAX.
C	1.778 (T.P.)	0.070 (T.P.)
D	0.50±0.10	0.020 <sup>+0.004</sup> <sub>-0.005</sub>
F	0.9 MIN.	0.035 MIN.
G	3.2±0.3	0.126±0.012
H	0.51 MIN.	0.020 MIN.
I	4.05 <sup>+0.26</sup> <sub>-0.20</sub>	0.159 <sup>+0.011</sup> <sub>-0.008</sub>
J	5.08 MAX.	0.200 MAX.
K	19.05 (T.P.)	0.750 (T.P.)
L	17.0±0.2	0.669 <sup>+0.009</sup> <sub>-0.008</sub>
M	0.25 <sup>+0.10</sup> <sub>-0.05</sub>	0.010 <sup>+0.004</sup> <sub>-0.003</sub>
N	0.17	0.007
R	0 to 15°	0 to 15°

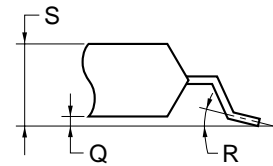
P64C-70-750A,C-3

**Remark** The package and material of ES products are the same as mass produced products.

64 PIN PLASTIC QFP (□14)



detail of lead end



NOTE

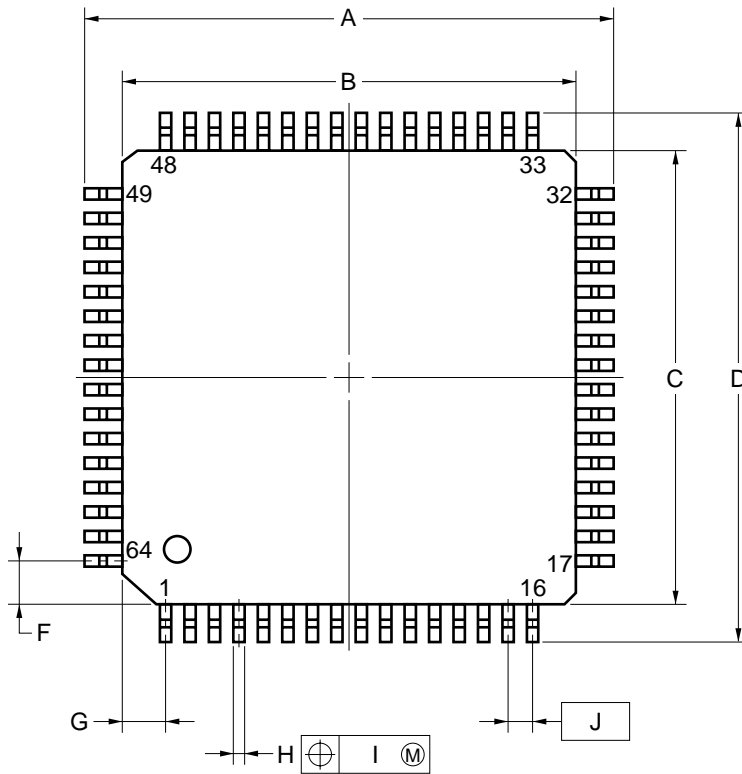
1. Controlling dimension — millimeter.
2. Each lead centerline is located within 0.15 mm (0.006 inch) of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS	INCHES
A	17.6±0.4	0.693±0.016
B	14.0±0.2	0.551 <sup>+0.009</sup> <sub>-0.008</sub>
C	14.0±0.2	0.551 <sup>+0.009</sup> <sub>-0.008</sub>
D	17.6±0.4	0.693±0.016
F	1.0	0.039
G	1.0	0.039
H	0.37 <sup>+0.08</sup> <sub>-0.07</sub>	0.015 <sup>+0.003</sup> <sub>-0.004</sub>
I	0.15	0.006
J	0.8 (T.P.)	0.031 (T.P.)
K	1.8±0.2	0.071±0.008
L	0.8±0.2	0.031 <sup>+0.009</sup> <sub>-0.008</sub>
M	0.17 <sup>+0.08</sup> <sub>-0.07</sub>	0.007 <sup>+0.003</sup> <sub>-0.004</sub>
N	0.10	0.004
P	2.55±0.1	0.100±0.004
Q	0.1±0.1	0.004±0.004
R	5°±5°	5°±5°
S	2.85 MAX.	0.113 MAX.

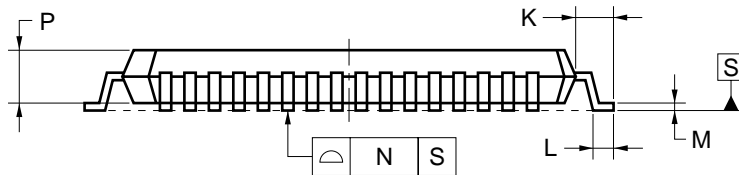
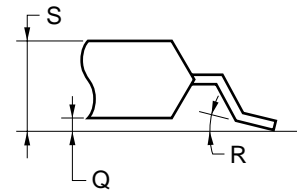
P64GC-80-AB8-4

**Remark** The package and material of ES products are the same as mass produced products.

64 PIN PLASTIC LQFP (12x12)



detail of lead end



ITEM	MILLIMETERS	INCHES
A	14.8±0.4	0.583±0.016
B	12.0±0.2	0.472 <sup>+0.009</sup> <sub>-0.008</sub>
C	12.0±0.2	0.472 <sup>+0.009</sup> <sub>-0.008</sub>
D	14.8±0.4	0.583±0.016
F	1.125	0.044
G	1.125	0.044
H	0.32±0.08	0.013 <sup>+0.003</sup> <sub>-0.004</sub>
I	0.13	0.005
J	0.65 (T.P.)	0.026
K	1.4±0.2	0.055±0.008
L	0.6±0.2	0.024 <sup>+0.008</sup> <sub>-0.009</sub>
M	0.17 <sup>+0.08</sup> <sub>-0.07</sub>	0.007 <sup>+0.003</sup> <sub>-0.004</sub>
N	0.10	0.004
P	1.4±0.1	0.055 <sup>+0.004</sup> <sub>-0.005</sub>
Q	0.125±0.075	0.005±0.003
R	5°±5°	5°±5°
S	1.7 MAX.	0.067 MAX.

P64GK-65-8A8-2

NOTES

- Controlling dimension — millimeter.
- Each lead centerline is located within 0.13 mm of its true position (T.P.) at maximum material condition.

**Remark** The package and material of ES products are the same as mass produced products.

**7. RECOMMENDED SOLDERING CONDITIONS**

The μPD78F0034A should be soldered and mounted under the following recommended conditions.

For the details of the recommended soldering conditions, refer to the document **Semiconductor Device Mounting Technology Manual (C10535E)**.

For soldering methods and conditions other than those recommended below, contact your NEC sales representative.

**Table 7-1. Surface Mounting Type Soldering Conditions**

**(1) μPD78F0034AGC-AB8: 64-pin plastic QFP (14 × 14 mm)**

Soldering Method	Soldering Conditions	Recommended Condition Symbol
Infrared reflow	Package peak temperature: 235°C, Time: 30 seconds Max. (at 210°C or higher), Count: Two times or less	IR35-00-2
VPS	Package peak temperature: 215°C, Time: 40 seconds Max. (at 200°C or higher), Count: Two times or less	VP15-00-2
Wave soldering	Solder bath temperature: 260°C Max., Time: 10 seconds Max., Count: Once, Preheating temperature: 120°C Max. (package surface temperature)	WS60-00-1
Partial heating	Pin temperature: 300°C Max., Time: 3 seconds Max. (per pin row)	–

**Caution Do not use different soldering methods together (except for partial heating).**

**(2) μPD78F0034AGK-8A8: 64-pin plastic LQFP (12 × 12 mm)**

Soldering Method	Soldering Conditions	Recommended Condition Symbol
Infrared reflow	Package peak temperature: 235°C, Time: 30 seconds Max. (at 210°C or higher), Count: Two times or less, Exposure limit: 7 days <sup>Note</sup> (after 7 days, prebake at 125°C for 10 hours)	IR35-107-2
VPS	Package peak temperature: 215°C, Time: 40 seconds Max. (at 200°C or higher), Count: Two times or less, Exposure limit: 7 days <sup>Note</sup> (after 7 days, prebake at 125°C for 10 hours)	VP15-107-2
Wave soldering	Solder bath temperature: 260°C Max., Time: 10 seconds Max., Count: Once, Preheating temperature: 120°C Max. (package surface temperature) Exposure limit: 7 days <sup>Note</sup> (after 7 days, prebake at 125°C for 10 hours)	WS60-107-1
Partial heating	Pin temperature: 300°C Max., Time: 3 seconds Max. (per pin row)	–

**Note** After opening the dry pack, store it at 25°C or less and 65% RH or less for the allowable storage period.

**Caution Do not use different soldering methods together (except for partial heating).**

Table 7-2. Through-Hole Type Soldering Conditions

μPD78F0034ACW: 64-pin plastic shrink DIP (750 mils)

Soldering Method	Soldering Conditions
Wave soldering (pin only)	Solder bath temperature: 260°C Max., Time: 10 seconds Max.
Partial heating	Pin temperature: 300°C Max., Time: 3 seconds Max. (per pin row)

**Caution** Apply wave soldering only to the pins and be careful not to bring solder into direct contact with the package.

**APPENDIX A. DEVELOPMENT TOOLS**

The following development tools are available for system development using the μPD78F0034A Subseries. Also refer to **(5) Cautions on Using Development Tools**.

**(1) Language Processing Software**

RA78K/0	Assembler package common to 78K/0 Series
CC78K/0	C compiler package common to 78K/0 Series
DF780034	Device file for μPD780034A Subseries
CC78K/0-L	C compiler library source file common to 78K/0 Series

**(2) Flash Memory Writing Tools**

Flashpro II (type No. FL-PR2), Flashpro III (type No. FL-PR3, PG-FP3)	Flash programmer dedicated to microcontrollers with on-chip flash memory
FA-64CW, FA-64GC, FA-64GK <sup>Note</sup>	Adapter for flash memory writing

**Note** Under development

**(3) Debugging Tools**

**When IE-78K0-NS in-circuit emulator is used**

IE-78K0-NS	In-circuit emulator common to 78K/0 Series
IE-70000-MC-PS-B	Power supply unit for IE-78K0-NS
IE-78K0-NS-PA <sup>Note</sup>	Performance board that enhances and expands the IE-78K0-NS functions
IE-70000-98-IF-C	Interface adapter used when PD-9800 Series PC (except notebook type) is used as host machine (C bus supported)
IE-70000-CD-IF-A	PC card and interface cable when PC-9800 Series notebook PC is used as host machine (PCMCIA socket supported)
IE-70000-PC-IF-C	Interface adapter when using IBM PC/ATM or compatible as host machine (ISA bus supported)
IE-70000-PCI-IF	Adapter necessary when using PCI-bus incorporated personal computer as host machine
IE-780034-NS-EM1	Emulation board to emulate the μPD780034A Subseries
NP-64CW	Emulation probe for 64-pin plastic shrink DIP (CW type)
NP-64GC	Emulation probe for 64-pin plastic QFP (CG-AB8 type)
NP-64GK <sup>Note</sup>	Emulation probe for 64-pin plastic LQFP (CG-8A8 type)
TGK-064SBW	Conversion adapter to connect the NP-64GK and a target system board on which the 64-pin plastic LQFP (GC-8A8 type) can be mounted
EV-9200GC-64	Socket mounted on target system board for the 64-pin plastic QFP (GC-AB8 type)
ID78K0-NS	Integrated debugger for IE-78K0-NS
SM78K0	System simulator common to 78K/0 Series
DF780034	Device file for μPD780034A Subseries

**Note** Under development

**When using in-circuit emulator IE-78001-R-A**

IE-78001-R-A	In-circuit emulator common to 78K/0 Series
IE-70000-98-IF-C	Interface adapter when using PC-9800 series as host machine (excluding notebook PCs) (C bus supported)
IE-70000-PC-IF-C	Interface adapter when using IBM PC/AT or compatible as host machine (ISA bus supported)
IE-70000-PCI-IF	Adapter necessary when using PCI-bus incorporated personal computers as host machine.
IE-78000-R-SV3	Interface adapter and cable when using EWS as host machine
IE-780034-NS-EM1	Emulation board to emulate $\mu$ PD780034A Subseries
IE-78K0-R-EX1	Emulation probe conversion board to use IE-780034-NS-EM1 on IE-78001-R-A
EP-78240CW-R	Emulation probe for 64-pin plastic shrink DIP (CW type)
EP-78240GC-R	Emulation probe for 64-pin plastic QFP (GC-AB8 type)
EP-78012GK-R	Emulation probe for 64-pin plastic LQFP (GK-8A8 type)
TGK-064SBW	Conversion adapter for connecting target system board designed to allow mounting of 64-pin plastic LQFP (GK-8A8) and NP-64GK.
EV-9200GC-64	Socket to be mounted on target system board manufactured for 64-pin plastic QFP (GC-AB8 type)
ID78K0	Integrated debugger for IE-78001-R-A
SM78K0	System simulator common to 78K/0 Series
DF780034	Device file for $\mu$ PD780034A Subseries

**(4) Real-time OS**

RX78K/0	Real-time OS for 78K/0 Series
MX78K0	OS for 78K/0 Series



**(5) Cautions on using development tools**

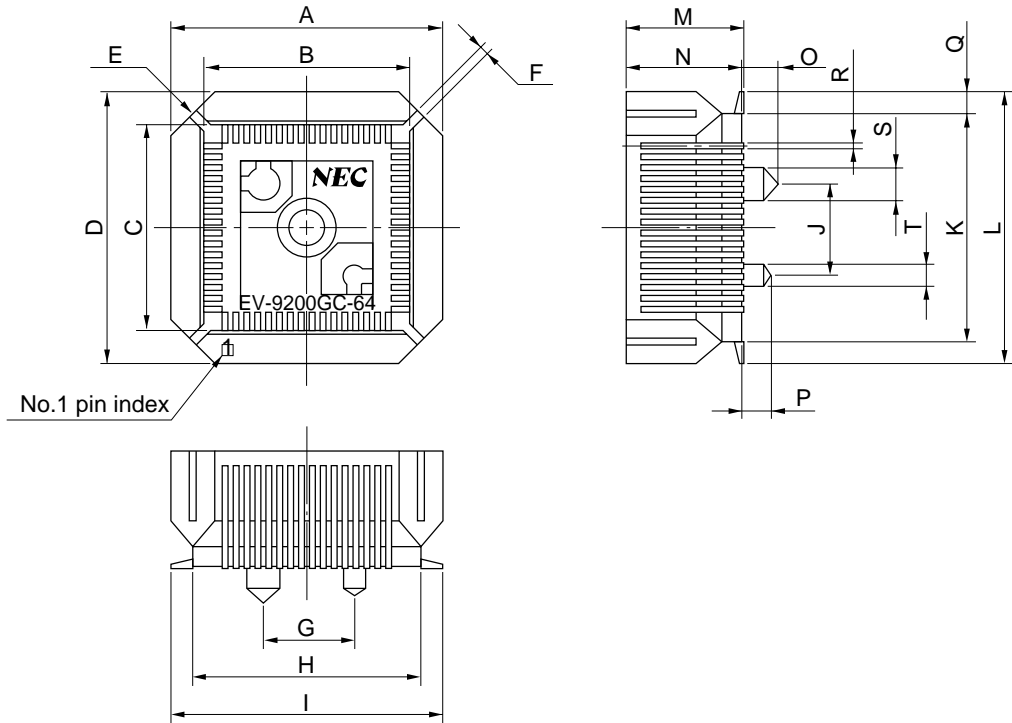
- The ID-78K0-NS, ID78K0, and SM78K0 are used in combination with the DF780034.
- The CC78K/0 and RX78K/0 are used in combination with the RA78K/0 and the DF780034.
- The FL-PR2, FL-PR3, FA-64CW, FA-64GC, FA64GK, NP-64CW, NP64GC, and NP-64GK are products made by Naito Densai Machida Mfg. Co., Ltd. (+81-44-822-3813).  
Contact an NEC distributor regarding the purchase of these products.
- The T GK-064SBW is a product made by TOKYO ELETECH CORPORATION.  
For further information contact Daimaru Kogyo, Ltd.  
Tokyo Electronic Division (+81-3-3820-7112)  
Osaka Electronic Division (+81-6-6244-6672)
- For third party development tools, see the **78K/0 Series Selection Guide (U11126E)**.
- The host machines and OSs supporting each software are as follows.

Software	Host Machine [OS]	PC	EWS
		PC-9800 series [Windows™] IBM PC/AT or compatibles [Japanese/English Windows]	HP9000 series 700™ [HP-UX™] SPARCstation™ [SunOS™, Solaris™] NEWS™ (RISC) [NEWS-OS™]
RA78K/0		√ <b>Note</b>	√
CC78K/0		√ <b>Note</b>	√
ID78K0-NS		√	—
ID78K0		√	√
SM78K0		√	—
RX78K/0		√ <b>Note</b>	√
MX78K0		√ <b>Note</b>	√

**Note** DOS-based software

Conversion Socket Drawing (EV-9200GC-64) and Footprints

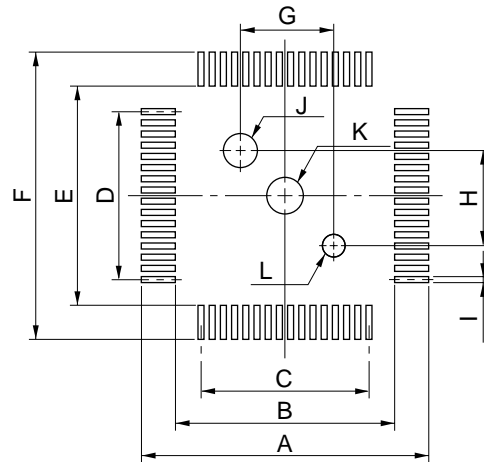
Figure A-1. EV-9200GC-64 Drawing (For Reference Only)



EV-9200GC-64-G0

ITEM	MILLIMETERS	INCHES
A	18.8	0.74
B	14.1	0.555
C	14.1	0.555
D	18.8	0.74
E	4-C 3.0	4-C 0.118
F	0.8	0.031
G	6.0	0.236
H	15.8	0.622
I	18.5	0.728
J	6.0	0.236
K	15.8	0.622
L	18.5	0.728
M	8.0	0.315
N	7.8	0.307
O	2.5	0.098
P	2.0	0.079
Q	1.35	0.053
R	0.35±0.1	0.014 <sup>+0.004</sup> <sub>-0.005</sub>
S	φ2.3	φ0.091
T	φ1.5	φ0.059

Figure A-2. EV-9200GC-64 Footprints (For Reference Only)



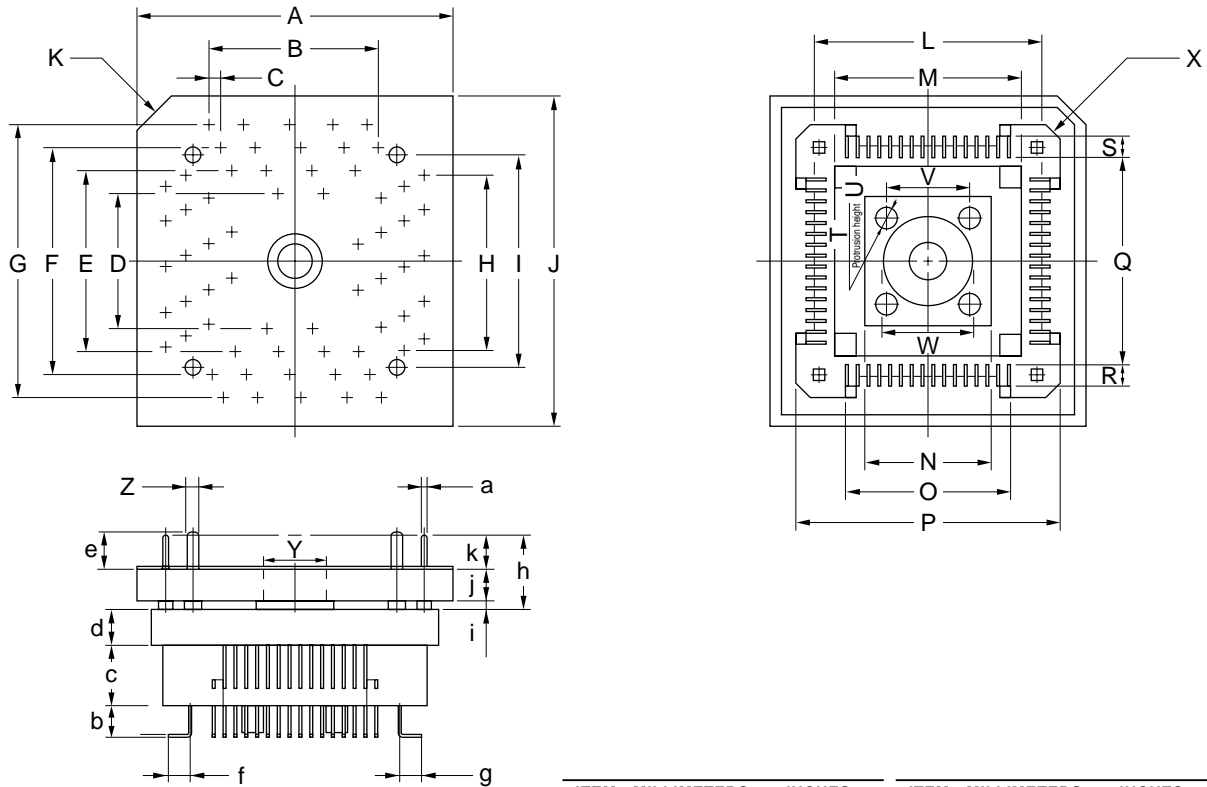
EV-9200GC-64-P1E

ITEM	MILLIMETERS	INCHES
A	19.5	0.768
B	14.8	0.583
C	$0.8 \pm 0.02 \times 15 = 12.0 \pm 0.05$	$0.031^{+0.002}_{-0.001} \times 0.591 = 0.472^{+0.003}_{-0.002}$
D	$0.8 \pm 0.02 \times 15 = 12.0 \pm 0.05$	$0.031^{+0.002}_{-0.001} \times 0.591 = 0.472^{+0.003}_{-0.002}$
E	14.8	0.583
F	19.5	0.768
G	$6.00 \pm 0.08$	$0.236^{+0.004}_{-0.003}$
H	$6.00 \pm 0.08$	$0.236^{+0.004}_{-0.003}$
I	$0.5 \pm 0.02$	$0.197^{+0.001}_{-0.002}$
J	$\phi 2.36 \pm 0.03$	$\phi 0.093^{+0.001}_{-0.002}$
K	$\phi 2.2 \pm 0.1$	$\phi 0.087^{+0.004}_{-0.005}$
L	$\phi 1.57 \pm 0.03$	$\phi 0.062^{+0.001}_{-0.002}$

**Caution** Dimensions of mount pad for EV-9200 and that for target device (QFP) may be different in some parts. For the recommended mount pad dimensions for QFP, refer to "SEMICONDUCTOR DEVICE MOUNTING TECHNOLOGY MANUAL" (C10535E).

Conversion Adapter Drawing (TGK-064SBW)

Figure A-3. TGK-064SBW Drawing (For Reference Only)



ITEM	MILLIMETERS	INCHES	ITEM	MILLIMETERS	INCHES
A	18.4	0.724	a	φ0.3	φ0.012
B	0.65x15=9.75	0.026x0.591=0.384	b	1.85	0.073
C	0.65	0.026	c	3.5	0.138
D	7.75	0.305	d	2.0	0.079
E	10.15	0.400	e	3.9	0.154
F	12.55	0.494	f	1.325	0.052
G	14.95	0.589	g	1.325	0.052
H	0.65x15=9.75	0.026x0.591=0.384	h	5.9	0.232
I	11.85	0.467	i	0.8	0.031
J	18.4	0.724	j	2.4	0.094
K	C 2.0	C 0.079	k	2.7	0.106
L	12.45	0.490	<b>TGK-064SBW-G0E</b>		
M	10.25	0.404			
N	7.7	0.303			
O	10.02	0.394			
P	14.92	0.587			
Q	11.1	0.437			
R	1.45	0.057			
S	1.45	0.057			
T	4-φ1.3	4-φ0.051			
U	1.8	0.071			
V	5.0	0.197			
W	φ5.3	φ0.209			
X	4-C 1.0	4-C 0.039			
Y	φ3.55	φ0.140			
Z	φ0.9	φ0.035			

Note: Product made by TOKYO ELETECH CORPORATION.

**APPENDIX B. RELATED DOCUMENTS**

**Device Related Documents**

Document Name	Document No. (English)	Document No. (Japanese)
μPD780024A, 780034A, 780024AY, 780034AY Subseries User's Manual	Under preparation	U14046J
μPD780031A, 780032A, 780033A, 780034A Data Sheet	U14044E	U14044J
μPD78F0034A Data Sheet	This manual	U14040J
78K/0 Series User's Manual Instruction	U12326E	U12326J
78K/0 Series Instruction Table	—	U10903J
78K/0 Series Instruction Set	—	U10904J

**Development Tool Documents (User's Manuals)**

Document Name	Document No. (English)	Document No. (Japanese)	
RA78K0 Assembler Package	Operation	U11802E	U11802J
	Assembly Language	U11801E	U11801J
	Structured Assembly Language	U11789E	U11789J
RA78K Series Structured Assembler Preprocessor	EEU-1402	U12323J	
CC78K/0 C Compiler	Operation	U11517E	U11517J
	Language	U11518E	U11518J
CC78K/0 C Compiler Application Note	Programming Know-how	U13034E	U13034J
IE-78K0-NS	To be prepared	To be prepared	
IE-78001-R-A	To be prepared	To be prepared	
IE-780034-NS-EM1	To be prepared	To be prepared	
EP-78240	U10332E	EEU-986	
EP-78012GK-R	EEU-1538	EEU-5012	
SM78K0 System Simulator-Windows based	Reference	U10181E	U10181J
SM78K Series System Simulator	External Part User Open Interface Specifications	U10092E	U10092J
ID78K0-NS Integrated Debugger Windows based	Reference	U12900E	U12900J
ID78K0 Integrated Debugger EWS based	Reference	—	U11151J
ID78K0 Integrated Debugger PC based	Reference	U11539E	U11539J
ID78K0 Integrated Debugger Windows based	Guide	U11649E	U11649J

**Caution** The above related documents are subject to change without notice. Be sure to read the latest documents before designing.

**Embedded Software Documents (User's Manuals)**

Document Name		Document No. (English)	Document No. (Japanese)
78K/0 Series Real-time OS	Basics	U11537E	U11537J
	Installation	U11536E	U11536J
78K/0 Series OS MX78K0	Basics	U12257E	U12257J

**Other Documents**

Document Name	Document No. (English)	Document No. (Japanese)
SEMICONDUCTORS SELECTION GUIDE Products & Packages (CD-ROM)	X13769X	
Semiconductor Device Mounting Technology Manual	C10535E	C10535J
Quality Grades on NEC Semiconductor Devices	C11531E	C11531J
NEC Semiconductor Device Reliability/Quality Control System	C10983E	C10983J
Guide to Prevent Damage for Semiconductor Devices by Electrostatic Discharge (ESD)	C11892E	C11892J
Microcomputer - Related Products by Third Party	—	U11416J

**Caution** The above related documents are subject to change without notice. Be sure to read the latest documents before designing.

[MEMO]

[MEMO]



[MEMO]

**NOTES FOR CMOS DEVICES****① PRECAUTION AGAINST ESD FOR SEMICONDUCTORS**

Note:

Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.

**② HANDLING OF UNUSED INPUT PINS FOR CMOS**

Note:

No connection for CMOS device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to  $V_{DD}$  or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.

**③ STATUS BEFORE INITIALIZATION OF MOS DEVICES**

Note:

Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for devices having reset function.

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- Device availability
- Ordering information
- Product release schedule
- Availability of related technical literature
- Development environment specifications (for example, specifications for third-party tools and components, host computers, power plugs, AC supply voltages, and so forth)
- Network requirements

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