

High Speed 512K x 8Bit CMOS Dynamic RAM with with Fast Page Mode

DESCRIPTION

This is a family of 524,288 x 8 bit Extended Data Out Mode CMOS DRAMs. Extended Data Out Mode offers high speed random access of memory cells within the same row. Access time (-4), power consumption(Normal or Low power) and package type(SOJ or TSOP-II) are optional features of this family. All of this family have $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ refresh, $\overline{\text{RAS}}$ -only refresh and Hidden refresh capabilities. Furthermore, Self-refresh operation is available in L-version. This 512Kx8 EDO Mode DRAM family is fabricated using Samsung's advanced CMOS process to realize high band-width, low power consumption and high reliability. It may be used as main memory unit for microcomputer, personal computer and portable machines.

FEATURES

• **Part Identification**

- KM48C512D/DL (5V, 1K Ref.)

• **Active Power Dissipation**

Unit : mW

Speed	Active Power Dissipation
-4	770

• **Refresh Cycles**

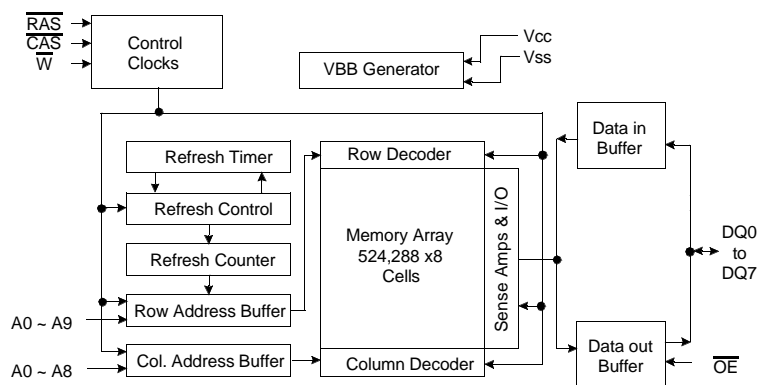
Part NO.	V _{CC}	Refresh cycle	Refresh period	
			Normal	L-ver
C512D	5V	1K	16ms	128ms

• **Performance Range**

Speed	t _{RAC}	t _{CAC}	t _{RC}	t _{PC}
-4	40ns	12ns	75ns	28ns

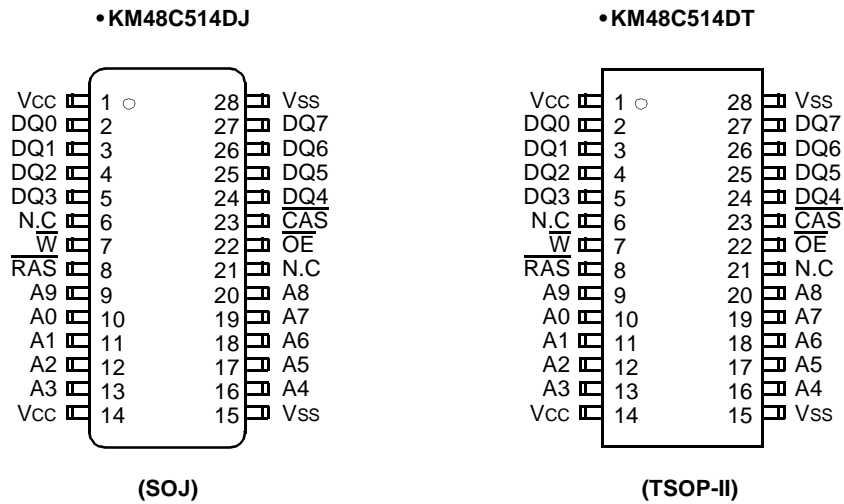
- Fast Page Mode operation
- Byte Read/Write operation
- $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ refresh capability
- $\overline{\text{RAS}}$ -only and Hidden refresh capability
- Self-refresh capability (L-ver only)
- TTL compatible inputs and outputs
- Early Write or output enable controlled write
- JEDEC Standard pinout
- Available in 28-pin SOJ 400mil & 28-pin TSOP(II) 400mil packages
- Dual +5V±10% power supply

FUNCTIONAL BLOCK DIAGRAM



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PIN CONFIGURATION (Top Views)



Pin Name	Pin Function
A0 - A9	Address Inputs
DQ0 - 7	Data In/Out
Vss	Ground
$\overline{\text{RAS}}$	Row Address Strobe
$\overline{\text{CAS}}$	Column Address Strobe
$\overline{\text{W}}$	Read/Write Input
$\overline{\text{OE}}$	Data Output Enable
Vcc	Power(+5V)
N.C	No Connection

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Rating	Units
Voltage on any pin relative to Vss	V _{IN} , V _{OUT}	-1.0 to +7.0	V
Voltage on Vcc supply relative to Vss	V _{CC}	-1.0 to +7.0	V
Storage Temperature	T _{stg}	-55 to +150	°C
Power Dissipation	P _D	1	W
Short Circuit Output Current	I _{OS}	50	mA

* Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltage referenced to Vss, T_A= 0 to 70°C)

Parameter	Symbol	Min	Typ	Max	Units
Supply Voltage	V _{CC}	4.5	5.0	5.5	V
Ground	V _{SS}	0	0	0	V
Input High Voltage	V _{IH}	2.4	-	V _{CC} +1.0* ¹	V
Input Low Voltage	V _{IL}	-1.0* ²	-	0.8	V

*1 : V_{CC}+2.0/20ns(5V), Pulse width is measured at V_{CC}

*2 : -2.0V/20ns(5V), Pulse width is measured at V_{SS}

DC AND OPERATING CHARACTERISTICS (Recommended operating conditions unless otherwise noted.)

Parameter	Symbol	Min	Max	Units
Input Leakage Current (Any input 0≤V _{IN} ≤V _{IN} +0.5V, all other input pins not under test=0 Volt)	I _{I(L)}	-5	5	uA
Output Leakage Current (Data out is disabled, 0V≤V _{OUT} ≤V _{CC})	I _{O(L)}	-5	5	uA
Output High Voltage Level(I _{OH} =-5mA)	V _{OH}	2.4	-	V
Output Low Voltage Level(I _{OL} =4.2mA)	V _{OL}	-	0.4	V

DC AND OPERATING CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.)

Symbol	Power	Max	Units
I _{CC1}	Don't care	140	mA
I _{CC2}	Don't care	2	mA
I _{CC3}	Don't care	140	mA
I _{CC4}	Don't care	110	mA
I _{CC5}	Normal L	1 150	mA uA
I _{CC6}	Don't care	140	mA
I _{CC7}	L	300	uA
I _{CCS}	L	200	uA

I_{CC1}* : Operating Current (\overline{RAS} and \overline{CAS} , Address cycling @trc=min.)

I_{CC2} : Standby Current ($\overline{RAS}=\overline{CAS}=\overline{W}=V_{IH}$)

I_{CC3}* : \overline{RAS} -only Refresh Current ($\overline{CAS}=V_{IH}$, \overline{RAS} , Address cycling @trc=min.)

I_{CC4}* : Fast Page Mode Current ($\overline{RAS}=V_{IL}$, \overline{CAS} , Address cycling @tpc=min.)

I_{CC5} : Standby Current ($\overline{RAS}=\overline{CAS}=\overline{W}=V_{CC}-0.2V$)

I_{CC6}* : \overline{CAS} -Before- \overline{RAS} Refresh Current (\overline{RAS} and \overline{CAS} cycling @trc=min.)

I_{CC7} : Battery back-up current, Average power supply current, Battery back-up mode

Input high voltage(V_{IH})= $V_{CC}-0.2V$, Input low voltage(V_{IL})= $0.2V$, $\overline{CAS}=0.2V$,

DQ=Don't care, $T_{RC}=31.25\mu s$, $T_{RAS}=T_{RASmin}\sim 300ns$

I_{CCS} : Self Refresh Current

$\overline{RAS}=\overline{CAS}=V_{IL}$, $\overline{W}=\overline{OE}=A0 \sim A9 =V_{CC}-0.2V$ or $0.2V$,

DQ0 ~ DQ7= $V_{CC}-0.2V$, $0.2V$ or Open

***Note :** I_{CC1}, I_{CC3}, I_{CC4} and I_{CC6} are dependent on output loading and cycle rates. Specified values are obtained with the output open. I_{CC} is specified as an average current. In I_{CC1}, I_{CC3}, I_{CC6} and I_{CC7}, address can be changed maximum once while $\overline{RAS}=V_{IL}$. In I_{CC4}, address can be changed maximum once within one fast page mode cycle time, t_{pc}.

CAPACITANCE ($T_A=25^\circ\text{C}$, $V_{CC}=5\text{V}$, $f=1\text{MHz}$)

Parameter	Symbol	Min	Max	Units
Input capacitance [A0 ~ A9]	CIN1	-	5	pF
Input capacitance [$\overline{\text{RAS}}$, $\overline{\text{CAS}}$, $\overline{\text{W}}$, $\overline{\text{OE}}$]	CIN2	-	7	pF
Output capacitance [DQ0 - DQ7]	CDQ	-	7	pF

AC CHARACTERISTICS ($0^\circ\text{C} \leq T_A \leq 60^\circ\text{C}$, See note 1,2)

Test condition : $V_{CC}=5.0\text{V} \pm 10\%$, $V_{ih}/V_{il}=2.8/0.4\text{V}$, $V_{oh}/V_{ol}=2.0/0.8\text{V}$

Parameter	Symbol	-4		Units	Notes
		Min	Max		
Random read or write cycle time	tRC	75		ns	
Read-modify-write cycle time	tRWC	111		ns	
Access time from $\overline{\text{RAS}}$	tRAC		40	ns	3,4,10
Access time from $\overline{\text{CAS}}$	tCAC		12	ns	3,4,5
Access time from column address	tAA		20	ns	3,10
$\overline{\text{CAS}}$ to output in Low-Z	tCLZ	0		ns	3
Output buffer turn-off delay	tOFF	0	9	ns	6
Transition time (rise and fall)	tT	3	50	ns	2
$\overline{\text{RAS}}$ precharge time	tRP	25		ns	
$\overline{\text{RAS}}$ pulse width	tRAS	40	10K	ns	
$\overline{\text{RAS}}$ hold time	tRSH	12		ns	
$\overline{\text{CAS}}$ hold time	tCSH	40		ns	
$\overline{\text{CAS}}$ pulse width	tCAS	12	10K	ns	
$\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ delay time	tRCD	18	28	ns	4
$\overline{\text{RAS}}$ to column address delay time	tRAD	13	20	ns	10
$\overline{\text{CAS}}$ to $\overline{\text{RAS}}$ precharge time	tCRP	5		ns	
Row address set-up time	tASR	0		ns	
Row address hold time	tRAH	8		ns	
Column address set-up time	tASC	0		ns	
Column address hold time	tCAH	10		ns	
Column address to $\overline{\text{RAS}}$ lead time	tRAL	20		ns	
Read command set-up time	tRCS	0		ns	
Read command hold time referenced to $\overline{\text{CAS}}$	tRCH	0		ns	8
Read command hold time referenced to $\overline{\text{RAS}}$	tRRH	0		ns	8
Write command set-up time	tWCS	0		ns	7
Write command hold time	tWCH	10		ns	
Write command pulse width	tWP	10		ns	
Write command to $\overline{\text{RAS}}$ lead time	tRWL	12		ns	
Write command to $\overline{\text{CAS}}$ lead time	tCWL	12		ns	

AC CHARACTERISTICS (Continued)

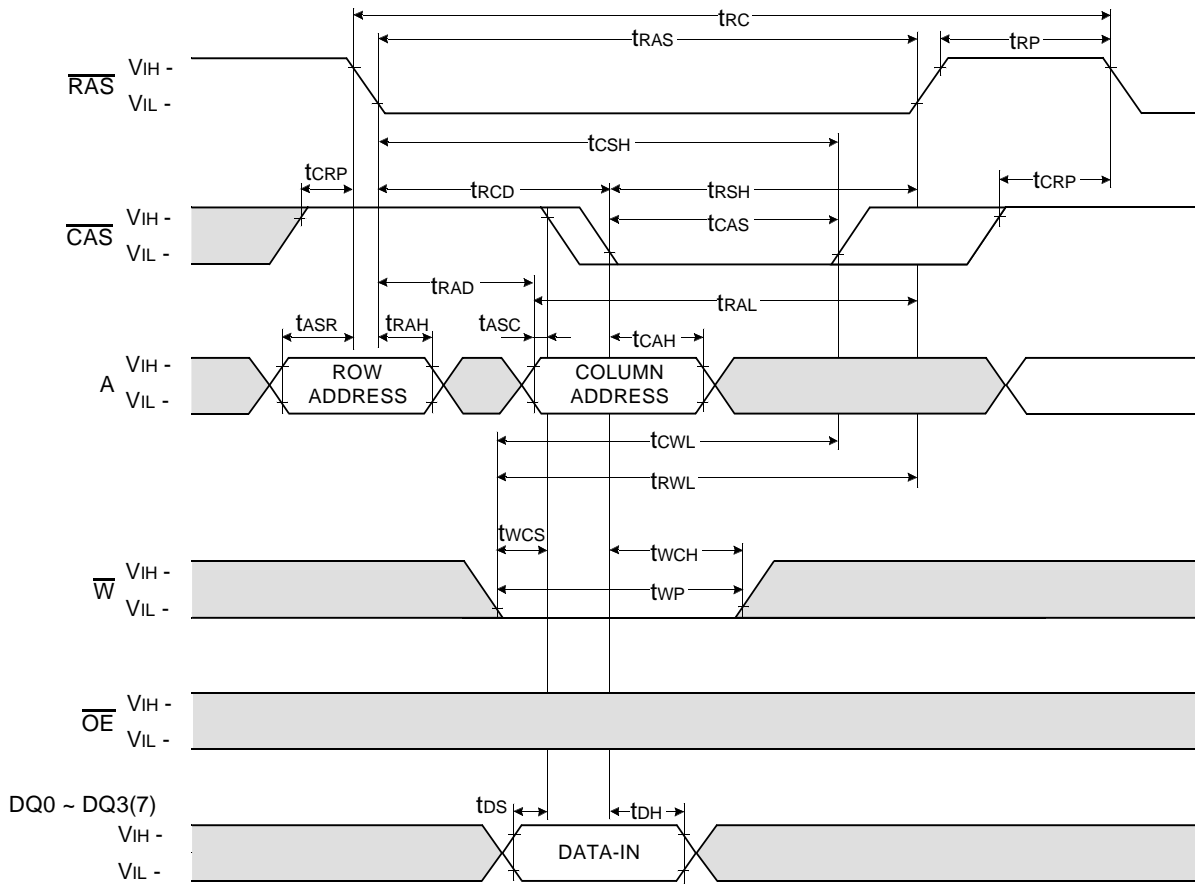
Parameter	Symbol	-4		Units	Notes
		Min	Max		
Data set-up time	tDS	0		ns	9
Data hold time	tDH	10		ns	9
Refresh period (Normal)	tREF		16	ms	
Refresh period (L-ver)	tREF		128	ms	
$\overline{\text{CAS}}$ to $\overline{\text{W}}$ delay time	tCWD	31		ns	7
$\overline{\text{RAS}}$ to $\overline{\text{W}}$ delay time	tRWD	59		ns	7
Column address $\overline{\text{W}}$ delay time	tAWD	39		ns	7
$\overline{\text{CAS}}$ precharge to $\overline{\text{W}}$ delay time	tCPWD	44		ns	7
$\overline{\text{CAS}}$ set-up time ($\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ refresh)	tCSR	10		ns	
$\overline{\text{CAS}}$ hold time ($\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ refresh)	tCHR	10		ns	
$\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ precharge time	tRPC	5		ns	
$\overline{\text{CAS}}$ precharge time ($\overline{\text{C}}$ -B- $\overline{\text{R}}$ counter test cycle)	tCPT	20		ns	
Access time from $\overline{\text{CAS}}$ precharge	tCPA		25	ns	3
Fast Page mode cycle time	tPC	28		ns	
Fast Page read-modify-write cycle time	tPRWC	67		ns	
$\overline{\text{CAS}}$ precharge time (Fast Page cycle)	tCP	6		ns	
$\overline{\text{RAS}}$ pulse width (Fast Page cycle)	tRASP	40	100K	ns	
$\overline{\text{RAS}}$ hold time from $\overline{\text{CAS}}$ precharge	tRHCP	23		ns	
$\overline{\text{OE}}$ access time	tOEA		12	ns	
$\overline{\text{OE}}$ to data delay	tOED	9		ns	
Output buffer turn off delay time from $\overline{\text{OE}}$	tOEZ	0	9	ns	6
$\overline{\text{OE}}$ command hold time	tOEH	12		ns	
$\overline{\text{RAS}}$ pulse width ($\overline{\text{C}}$ -B- $\overline{\text{R}}$ self refresh)	tRASS	100		us	11,12,13
$\overline{\text{RAS}}$ precharge time ($\overline{\text{C}}$ -B- $\overline{\text{R}}$ self refresh)	tRPS	74		ns	11,12,13
$\overline{\text{CAS}}$ hold time ($\overline{\text{C}}$ -B- $\overline{\text{R}}$ self refresh)	tCHS	-50		ns	11,12,13

NOTES

1. An initial pause of 200us is required after power-up followed by any $\overline{\text{RAS}}$ -only refresh or $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ refresh cycles before proper device operation is achieved.
2. $V_{IH}(\text{min})$ and $V_{IL}(\text{max})$ are reference levels for measuring timing of input signals.
Transition times are measured between $V_{IH}(\text{min})$ and $V_{IL}(\text{max})$ and are assumed to be 5ns for all inputs.
3. Measured with a load equivalent to 2 TTL load and 30pF. Dout reference level : $V_{oh}/V_{ol}=2.0V/0.8V$
4. Operation within the $t_{\text{RCD}}(\text{max})$ limit insures that $t_{\text{RAC}}(\text{max})$ can be met. $t_{\text{RCD}}(\text{max})$ is specified as a reference point only.
If t_{RCD} is greater than the specified $t_{\text{RCD}}(\text{max})$ limit, then access time is controlled exclusively by t_{CAC} .
5. Assumes that $t_{\text{RCD}} \geq t_{\text{RCD}}(\text{max})$.
6. This parameter defines the time at which the output achieves the open circuit condition and is not referenced to V_{oh} or V_{ol} .
7. t_{WCS} , t_{RWD} , t_{CWD} , t_{AWD} and t_{CPWD} are non restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If $t_{\text{WCS}} \geq t_{\text{WCS}}(\text{min})$, the cycle is an early write cycle and the data output will remain high impedance for the duration of the cycle. If $t_{\text{CWD}} \geq t_{\text{CWD}}(\text{min})$, $t_{\text{RWD}} \geq t_{\text{RWD}}(\text{min})$, $t_{\text{AWD}} \geq t_{\text{AWD}}(\text{min})$ and $t_{\text{CPWD}} \geq t_{\text{CPWD}}(\text{min})$ then the cycle is a read-modify-write cycle and the data output will contain the data read from the selected address. If neither of the above conditions is satisfied, the condition of the data out is indeterminate.
8. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
9. This parameters are referenced to $\overline{\text{CAS}}$ falling edge in early write cycles and to $\overline{\text{W}}$ falling edge in $\overline{\text{OE}}$ controlled write cycle and read-modify-write cycles.
10. Operation within the $t_{\text{RAD}}(\text{max})$ limit insures that $t_{\text{RAC}}(\text{max})$ can be met. $t_{\text{RAD}}(\text{max})$ is specified as a reference point only.
If t_{RAD} is greater than the specified $t_{\text{RAD}}(\text{max})$ limit, then access time is controlled by t_{AA} .
11. If $t_{\text{RASS}} \geq 100\text{us}$, then $\overline{\text{RAS}}$ precharge time must use t_{RPS} instead of t_{RP} .
12. For $\overline{\text{RAS}}$ -only refresh and burst $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ refresh mode, 1024(1K) cycle of burst refresh must be executed within 16ms before and after self refresh, in order to meet refresh specification.
13. For distributed $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ with 15.6us interval, $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ refresh should be executed with in 15.6us immediately before and after self refresh in order to meet refresh specification.

WRITE CYCLE (EARLY WRITE)

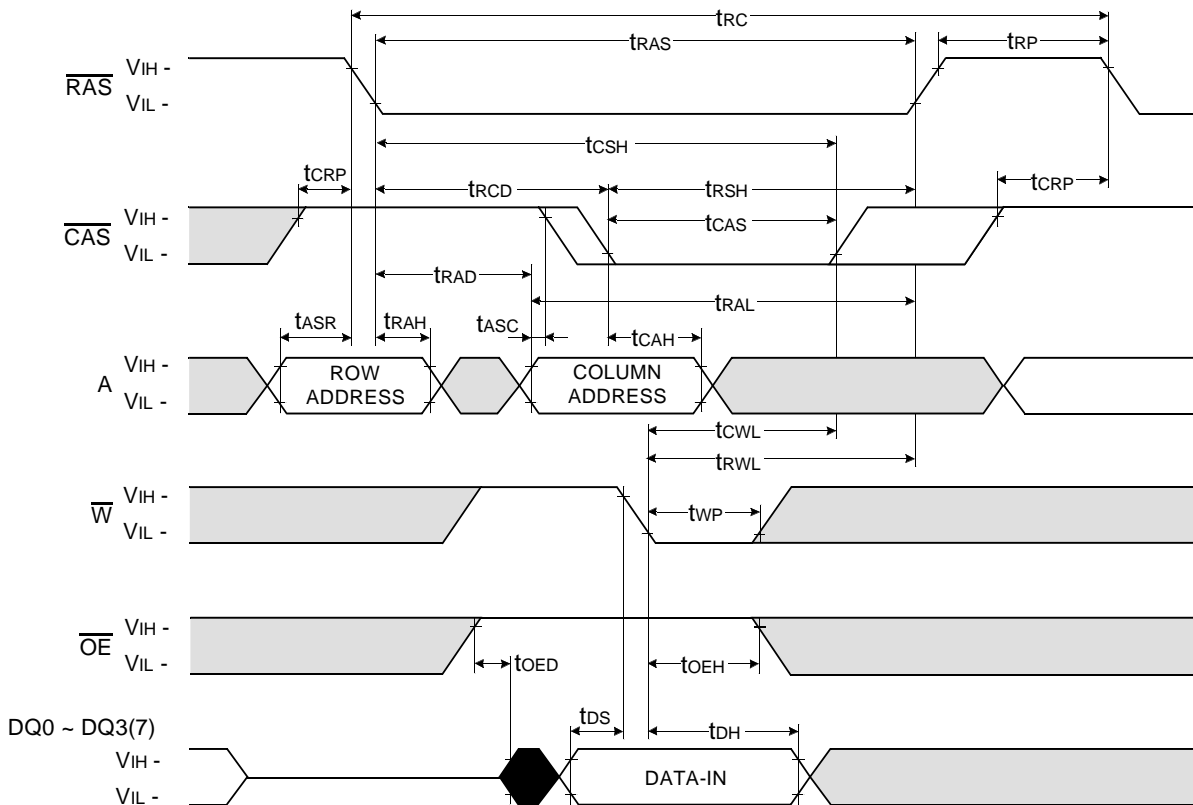
NOTE : DOUT = OPEN



□ Don't care
 ■ Undefined

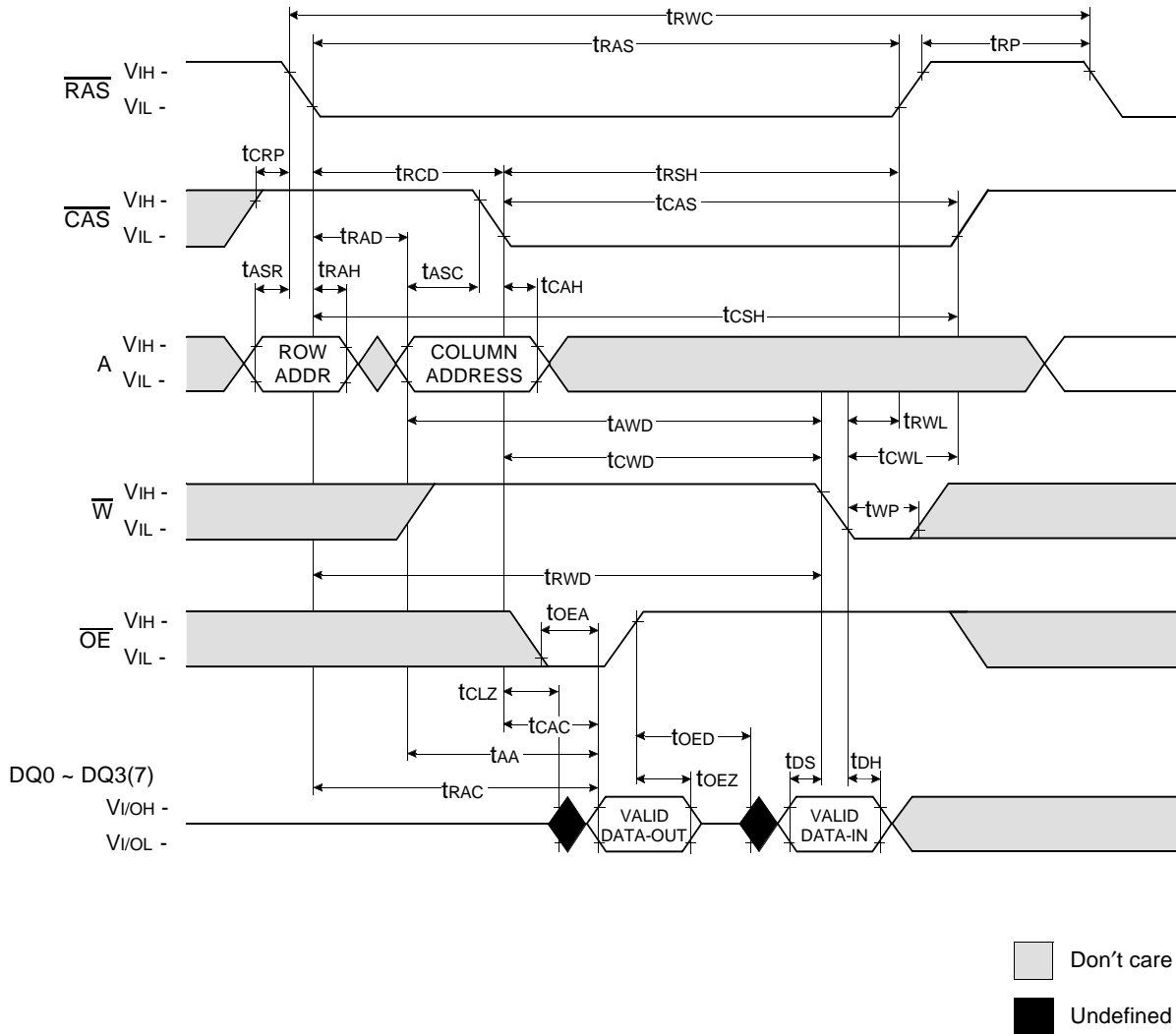
WRITE CYCLE (\overline{OE} CONTROLLED WRITE)

NOTE : DOUT = OPEN

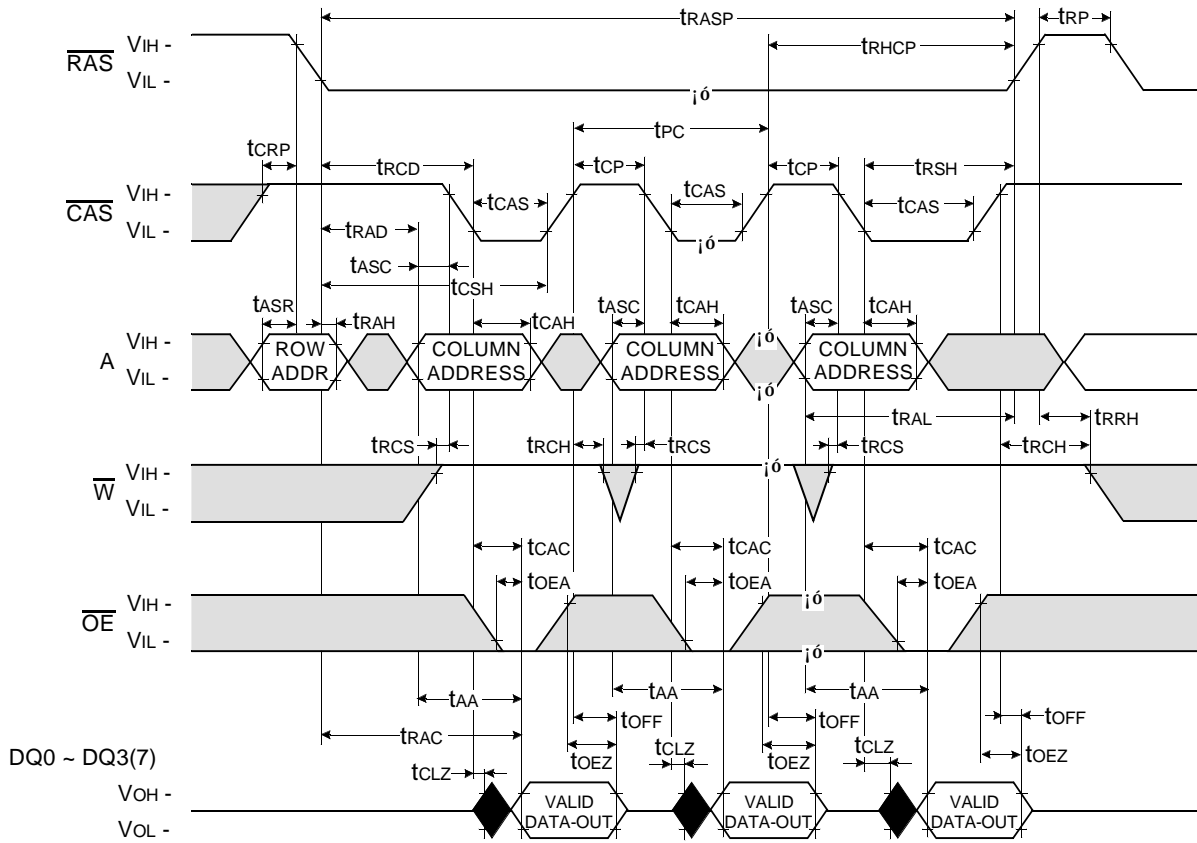


□ Don't care
 ■ Undefined

READ - MODIFY - WRITE CYCLE

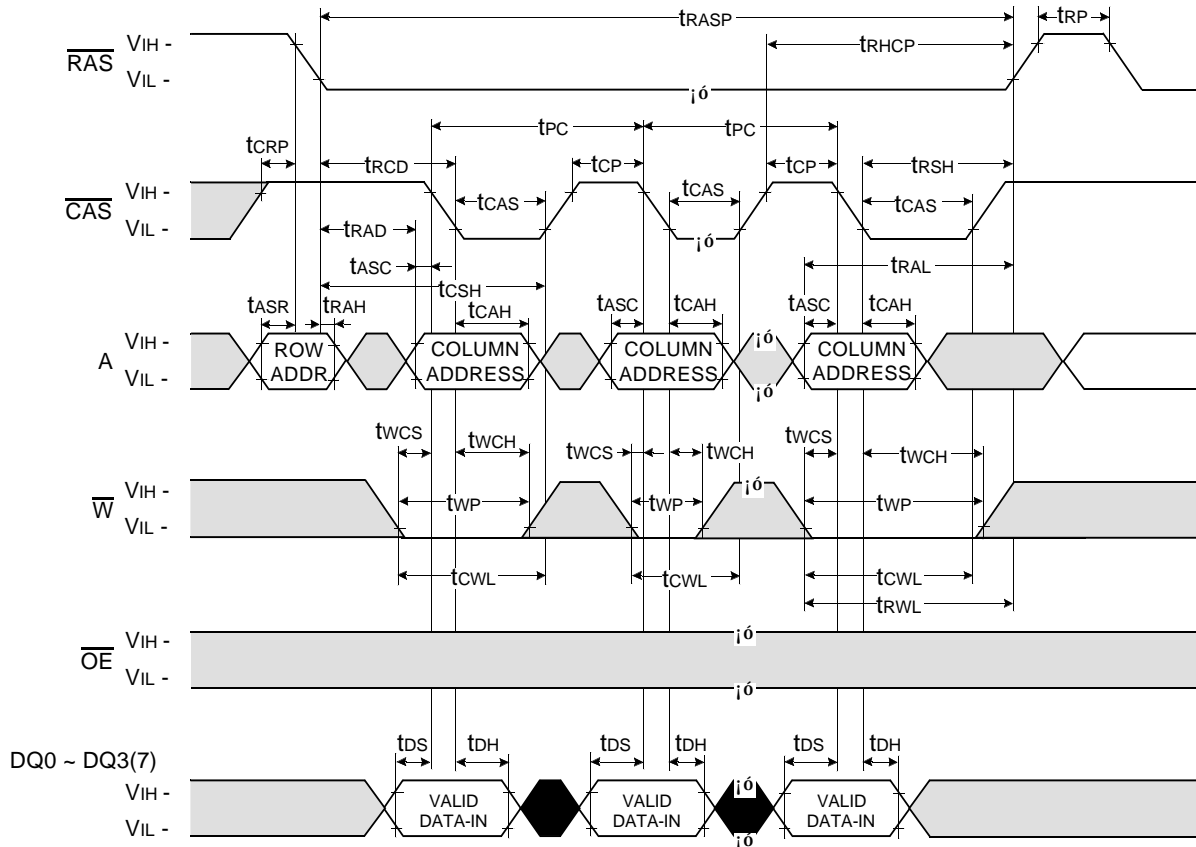


FAST PAGE READ CYCLE



FAST PAGE WRITE CYCLE (EARLY WRITE)

NOTE : DOUT = OPEN

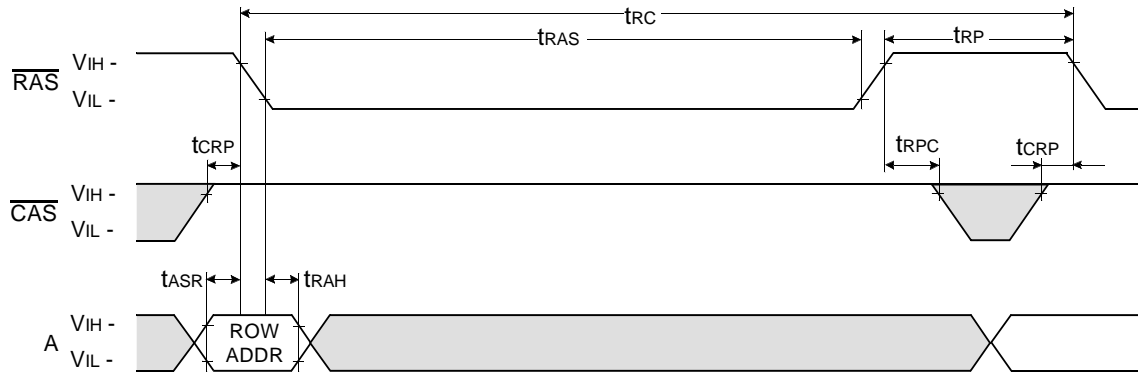


□ Don't care
 ■ Undefined

$\overline{\text{RAS}}$ - ONLY REFRESH CYCLE

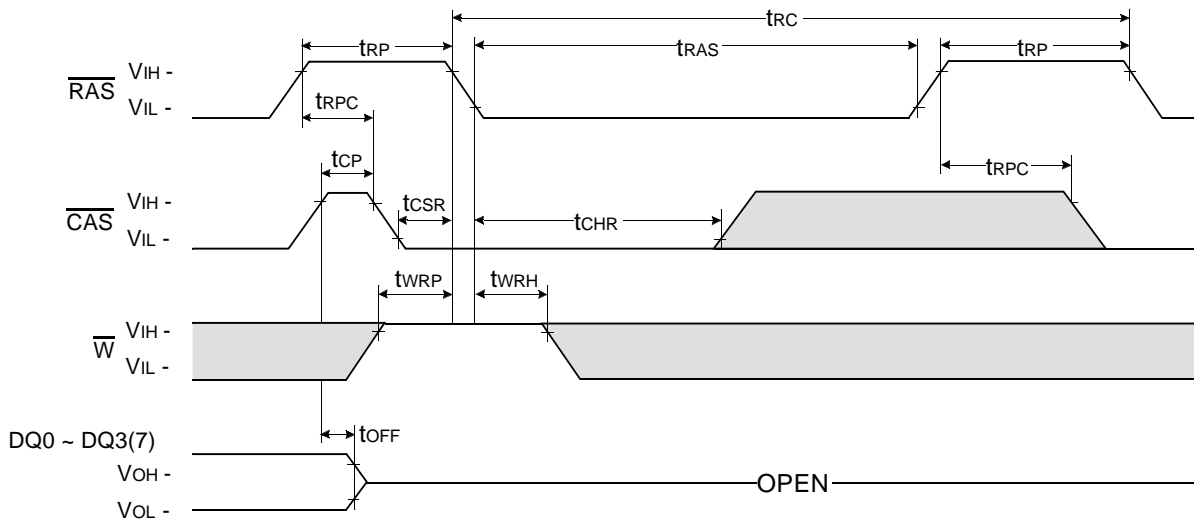
NOTE : $\overline{\text{W}}$, $\overline{\text{OE}}$, DIN = Don't care

DOUT = OPEN



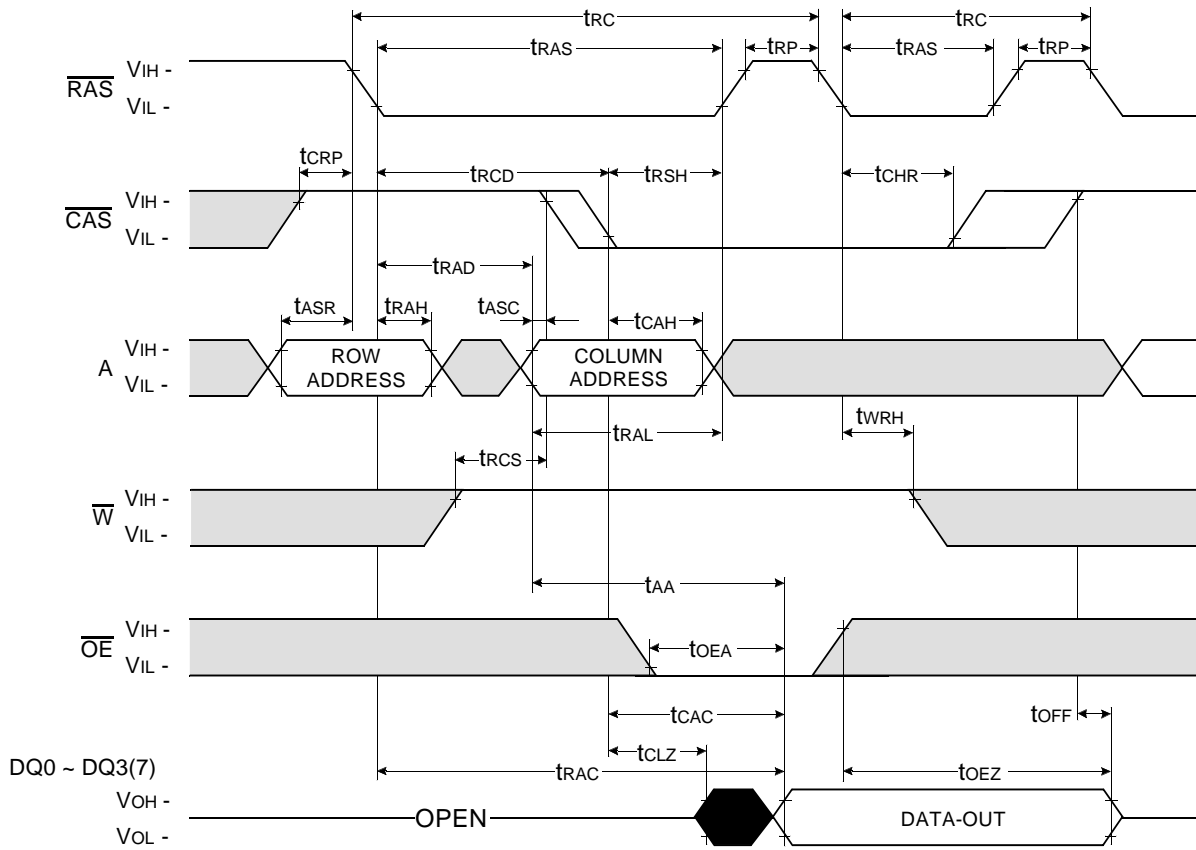
$\overline{\text{CAS}}$ - BEFORE - $\overline{\text{RAS}}$ REFRESH CYCLE

NOTE : $\overline{\text{OE}}$, A = Don't care



□ Don't care
 ■ Undefined

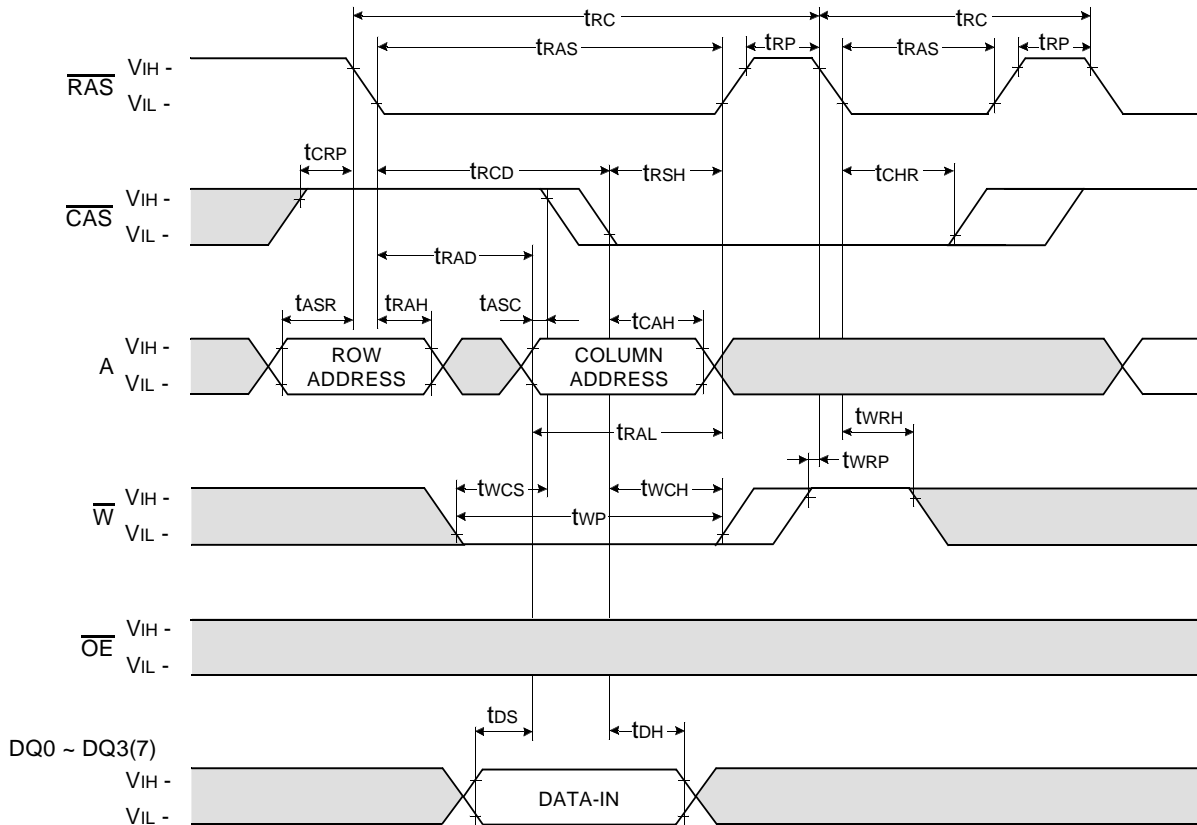
HIDDEN REFRESH CYCLE (READ)



□ Don't care
 ■ Undefined

HIDDEN REFRESH CYCLE (WRITE)

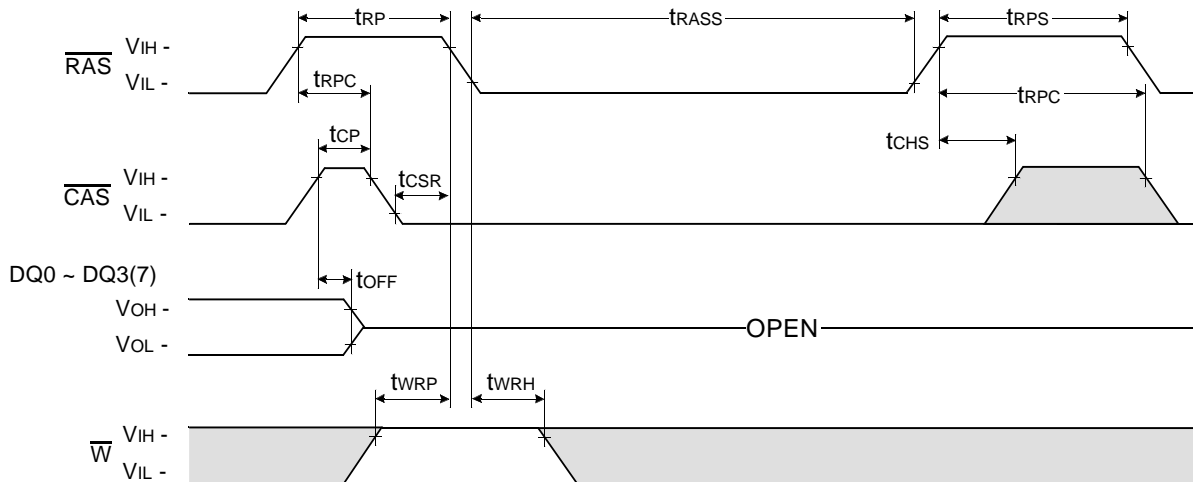
NOTE : DOUT = OPEN



□ Don't care
 ■ Undefined

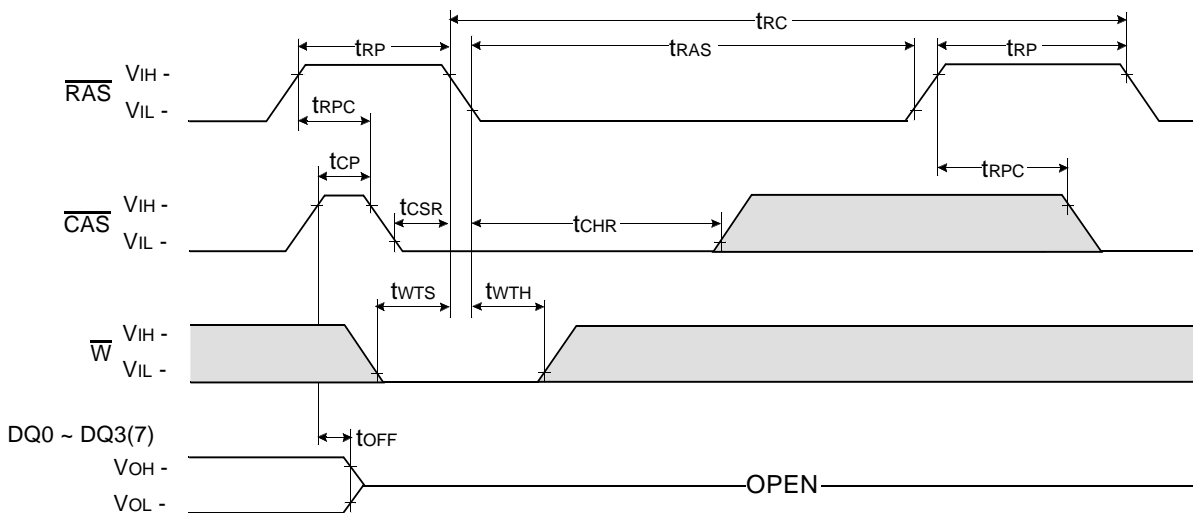
$\overline{\text{CAS}}$ - BEFORE - $\overline{\text{RAS}}$ SELF REFRESH CYCLE

NOTE : $\overline{\text{OE}}$, A = Don't care



TEST MODE IN CYCLE

NOTE : $\overline{\text{OE}}$, A = Don't care



□ Don't care
 ■ Undefined

PACKAGE DIMENSION

