10k ECL Programmable Delay Lines

GECLPG

- 10k ECL logic levels.
- 3-bit binary gives 7 equal step delays.
- Available in 10 step delays from 1 ns to 10 ns.
- Low inherent delay (To); To=3.0+1.5 ns
- Temperature range: -30 to +85^{o}C.
- Fanout: 70 ECL loads.
- MX model designates military models with temperature range -55 to +125^{o}C and ceramic package IC screened to MIL-STD-883C and 38510.
- Military models as “MX” above, but in-house burn-in and thermal shock, add suffix "MY."

MODEL GECLDL PROGRAMMABLE DELAY LINES

TECHNITROL PART NO.	Step Delay ns ± ns	Max. Delay ns ± ns	Output Rise Time Max. (ns)
GECLPG301MX	1.0 ± .4	10.0 ± 1.5	3.6
GECLPG302MX	2.0 ± .6	17.0 ± 1.5	3.6
GECLPG303MX	3.0 ± 1.0	24.0 ± 1.5	3.6
GECLPG304MX	4.0 ± 1.0	31.0 ± 2.0	3.6
GECLPG305MX	5.0 ± 1.5	38.0 ± 2.0	3.6
GECLPG306MX	6.0 ± 1.5	45.0 ± 2.5	3.6
GECLPG307MX	7.0 ± 1.5	52.0 ± 2.5	3.6
GECLPG308MX	8.0 ± 1.5	59.0 ± 3.0	3.6
GECLPG309MX	9.0 ± 1.5	66.0 ± 3.5	3.6
GECLPG310MX	10.0 ± 1.5	73.0 ± 3.0	3.6

- Delay Characteristics measured at V_{cc} = -5.2V ± .01 Vdc. T_a = 25^{o} C, no load.
- Delay Tolerance ±1.5 ns or 5%, whichever is greater.
- Delay time measured @ -1.3V.
- 500 linear FPM airflow and output terminated with 50 ohm to -2.0 Vdc.
- Rise time measured from 20 to 80% of output pulse.
- For minimum input pulse width -- contact factory.
- Input is internally terminated, therefore the delay line driver does not require a pulldown resistor.

SCHEMATIC

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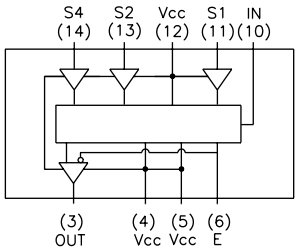
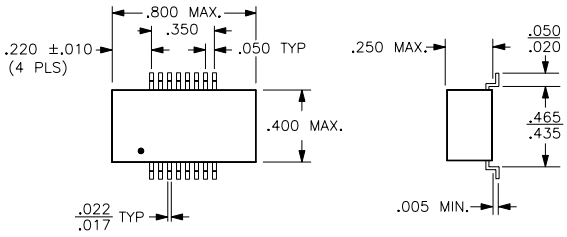


NOTE: ALL UNUSED PINS SHALL HAVE NO ELECTRICAL OR CAPACITIVE TYPE OF CONNECTION.

MECHANICAL OUTLINE



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Notes

- Pin numbers shown are for reference only and are not necessarily marked on unit.
- Lead material is electro tin plated (alloy 42) or solder dipped.
- All specifications are subject to change without notice.