Ordering number : ENN*6614A

CMOS IC

LC898023KW, 898023KL

40× Playback/16× Write CD-R/RW Encoder/Decoder IC with Built-in SCSI Interface

Preliminary

BURN-Proof™

Functions

- CD-ROM decoder/encoder functions
- CD decoder/encoder functions
- Pit and wobble CLV servo
- CAV audio functions
- SCSI interface (includes the register block)
- Subcode encoder/decoder functions
- ATIP demodulator/ATIP decoder
- Supports BURN-Proof recording
- Write strategy function (CD-R/RW)
- CD-DSP function with built-in digital servo

Features

- ECC and EDC correction/addition (decoding/encoding) for CD-ROM data.
- ECC error correction/addition (decoding/encoding) for subcode data
- Servo control implemented in a digital servo system (decoding/encoding)
- Wobble CLV servo control using ATIP data (encoding)
- ATIP decoding function and CRC check function (decoding/encoding)
- CIRC code generation and addition and EFM modulation (encoding)
- CAV audio functions
- Write strategy function supports 16× recording.
- Built-in SCSI interface (supports Ultra SCSI)
- Supports 40× decoding and 16× encoding.
  Clock frequencies: CD-ROM block: 33.8688 MHz, SCSI block: 20 MHz
- Ultra SCSI data transfer rate: 20 Mbyte/s (Maximum synchronous transfer rate), Fast SCSI: 10 Mbyte/s (Maximum synchronous transfer rate), 5 Mbyte/s (Maximum asynchronous transfer rate)
  Uses 16-bit data bus 45 ns EDO DRAM.
- From 1 to 64 Mbits of buffer RAM can be used. (16-bit data bus EDO DRAM)
- The user can freely set up the CD main channel, C2 flag, and subcode areas in buffer RAM.
- Batch transfer function (Function for transferring the CD main channel, C2 flag, subcode, and other data in a single operation)
- Multi-transfer function (Function for automatically transferring multiple blocks to the host in a single operation)

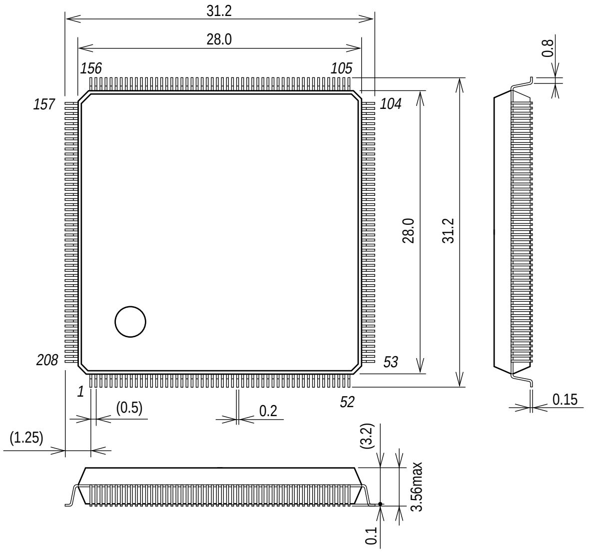
"BURN-Proof" stands for Proof against Buffer Under RuN error, not for proof against burning.
"BURN-Proof" is a trademark of SANYO Electric Co.,Ltd.

Package Dimensions

unit: mm

3261-SQFP208J (28 × 28)

[LC898023KW]

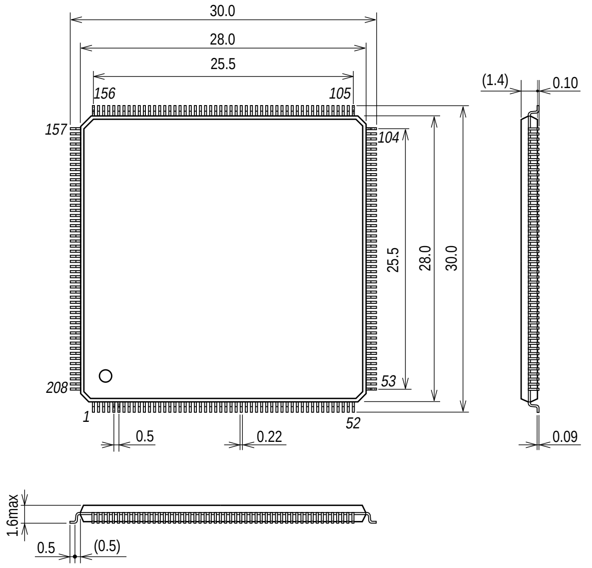


SANYO: SQFP208J (28 × 28)

unit: mm

3264-LQFP208

[LC898023KL]



SANYO: LQFP208

Specifications

Absolute Maximum Ratings at $V_{SS} = 0$ V

Parameter	Symbol	Conditions	Ratings	Unit
Supply voltage	$V_{DD}5$ max	Ta ≤ 25°C	–0.3 to +6.0	V
	$V_{DD}3$ max	Ta ≤ 25°C	–0.3 to +4.6	V
I/O voltages	V_I5, V_O5	Ta ≤ 25°C	–0.3 to $V_{DD}5$ + 0.3	V
	V_I3, V_O3	Ta ≤ 25°C	–0.3 to $V_{DD}3$ + 0.3	V
Allowable power dissipation	Pd max	Ta ≤ 70°C	900	mW
Operating temperature	Topr		–30 to +70	°C
Storage temperature	Tstg		–55 to +125	°C
Soldering conditions (pins only)		10 seconds	260	°C

Allowable Operating Ranges at Ta = –30 to +70°C, $V_{SS} = 0$ V

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
[I/O cells, 5.0 V power supply]						
Supply voltage	$V_{DD}5$		4.5	5.0	5.5	V
Input voltage range	V_{IN}		0		$V_{DD}5$	V
[Internal cells, 3.3 V power supply]						
Supply voltage	$V_{DD}3$		3.0	3.3	3.6	V
Input voltage range	V_{IN}		0		$V_{DD}3$	V

Electrical Characteristics at Ta = –30 to +70°C, V_{SS} = 0 V, V_{DD} = 4.5 to 5.5 V

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Input high-level voltage	V_{IH}	TTL level inputs: (2), (14)	2.2			V
Input low-level voltage	V_{IL}				0.8	V
Input high-level voltage	V_{IH}	TTL level inputs with built-in pull-up resistors: (13)	2.2			V
Input low-level voltage	V_{IL}				0.8	V
Input high-level voltage	V_{IH}	TTL level Schmitt trigger inputs: (1)	2.5			V
Input low-level voltage	V_{IL}				0.6	V
Input high-level voltage	V_{IH}	(15)	2.0			V
Input low-level voltage	V_{IL}				0.8	V
Input high-level voltage	V_{IH}	CMOS level Schmitt trigger inputs: (3)	0.8 V_{DD}			V
Input low-level voltage	V_{IL}				0.2 V_{DD}	V
Input high-level voltage	V_{IH}	CMOS level inputs with built-in pull-up resistors: (4)	0.7 V_{DD}			V
Input low-level voltage	V_{IL}				0.3 V_{DD}	V
Analog input voltage	V_{ANI}	(5)	1/4 V_{DD}		3/4 V_{DD}	V
Output high-level voltage	V_{OH}	I_{OH} = –12 mA: (8)	V_{DD} – 2.1			V
Output low-level voltage	V_{OL}	I_{OL} = 12 mA: (8)			0.4	V
Output high-level voltage	V_{OH}	I_{OH} = –8 mA: (7)	V_{DD} – 2.1			V
Output low-level voltage	V_{OL}	I_{OL} = 8 mA: (7)			0.4	V
Output high-level voltage	V_{OH}	I_{OH} = –2 mA: (6), (13), (14)	V_{DD} – 2.1			V
Output low-level voltage	V_{OL}	I_{OL} = 2 mA: (6), (13), (14)			0.4	V
Output low-level voltage	V_{OL}	I_{OL} = 48 mA: (15)			0.4	V
Output low-level voltage	V_{OL}	I_{OL} = 8 mA: (12)			0.4	V
Output low-level voltage	V_{OL}	I_{OL} = 1 mA: (9)			0.4	V
Output high-level voltage	V_{OH}	I_{OH} = –4 mA: (11)	V_{DD} – 2.1			V
Output low-level voltage	V_{OL}	I_{OL} = 4 mA: (11)			0.4	V
Output high-level voltage	V_{OH}	I_{OH} = –6 mA: (16), (17)	2.4			V
Output low-level voltage	V_{OL}	I_{OL} = 6 mA: (16), (17)			0.4	V
Analog output voltage	V_{ANO}	(10)	1/4 V_{DD}		3/4 V_{DD}	V
Input leakage current	I_{IL}	V_I = V_{SS}, V_{DD}: (1), (2), (14), (15)	–10		+10	µA
Output leakage current	I_{OZ}	In the high-impedance output state: (9), (11), (12)	–10		+10	µA
Pull-up resistance	R_{UP}	(12), (13)	40	80	160	kΩ
Pull-up resistance	R_{UP}	(4)	50	100	200	kΩ

The applicable pin groups are listed on the following page.

Applicable Pins

[INPUT]

(1) · · · · · WOBBLE, $\overline{\text{CS}}$, $\overline{\text{RD}}$, $\overline{\text{WR}}$, DEF, HFL, TES, $\overline{\text{RESET}}$
(2) · · · · · SUA0 to SUA7, TEST0 to TEST4
(3) · · · · · WRITE
(4) · · · · · FG
(5) · · · · · AD0, AD1, RREC, FE, TE, VREF, FR, OPP, JITIN, PCKISTF, PCKISTP, EFMIN, EFMIN2, SLCIST1, SLCIST2

[OUTPUT]

(6) · · · · · LDON
(7) · · · · · EFMG, SHOCK, LOCK, EFMO, SSP2/1, RAPC, WAPC, H11TO, LDH, ATEST3, ATEST1, WDAT, NWDAT
(8) · · · · · PCK2, SUBSYNC
(9) · · · · · PDS1 to PDS3
(10) · · · · DA0 to DA2, TDO, FDO, SLDO, SPDO, JITC, LOUT, ROUT, PDO, RPO, SLDO, SLCO1 to SLCO3
(11) · · · · DSLB
(12) · · · · $\overline{\text{INT0}}$, $\overline{\text{INT1}}$, $\overline{\text{SWAIT}}$
(16) · · · · RA0 to RA9, $\overline{\text{CAS0}}$ to $\overline{\text{CAS1}}$, $\overline{\text{RAS0}}$ to $\overline{\text{RAS2}}$, $\overline{\text{LWE}}$, $\overline{\text{UWE}}$, $\overline{\text{OE}}$

[INOUT]

(13) · · · · D0 to D7
(17) · · · · ID0 to ID15
(14) · · · · ATIPSYNC, BICLK, BIDATA, ACRCNG
(15) · · · · $\overline{\text{ACK}}$, $\overline{\text{ATN}}$, $\overline{\text{BSY}}$, C/D, $\overline{\text{DB0}}$ to $\overline{\text{DB7}}$, $\overline{\text{DBP}}$, I/O, $\overline{\text{MSG}}$, $\overline{\text{REQ}}$, $\overline{\text{RST}}$, $\overline{\text{SEL}}$

Note: The XTAL0, XTAL1, XTALCK0, and XTALCK1 are not included in the DC characteristics.

SCSI Pin Input Characteristics

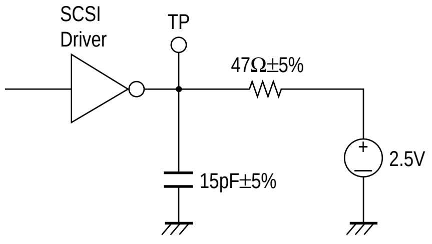
Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Input threshold voltage	V_{t+t1}	V_{DD} = 4.50 to 5.50 V		1.60	2.00	V
	V_{t-t1}	V_{DD} = 4.50 to 5.50 V	0.80	1.10		V
Hysteresis width	ΔV_{tt1}	V_{DD} = 5.0 V	0.41	0.5		

Active Negation Output Characteristics

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Output high voltage	V_{OH}		2.5			V
Output low voltage	V_{OL}				0.4	V

Note: The active negation output characteristics only applies to $\overline{\text{DB0}}$ to $\overline{\text{DB7}}$, $\overline{\text{REQ}}$, and $\overline{\text{DBPB}}$

Rise Time Test Circuit



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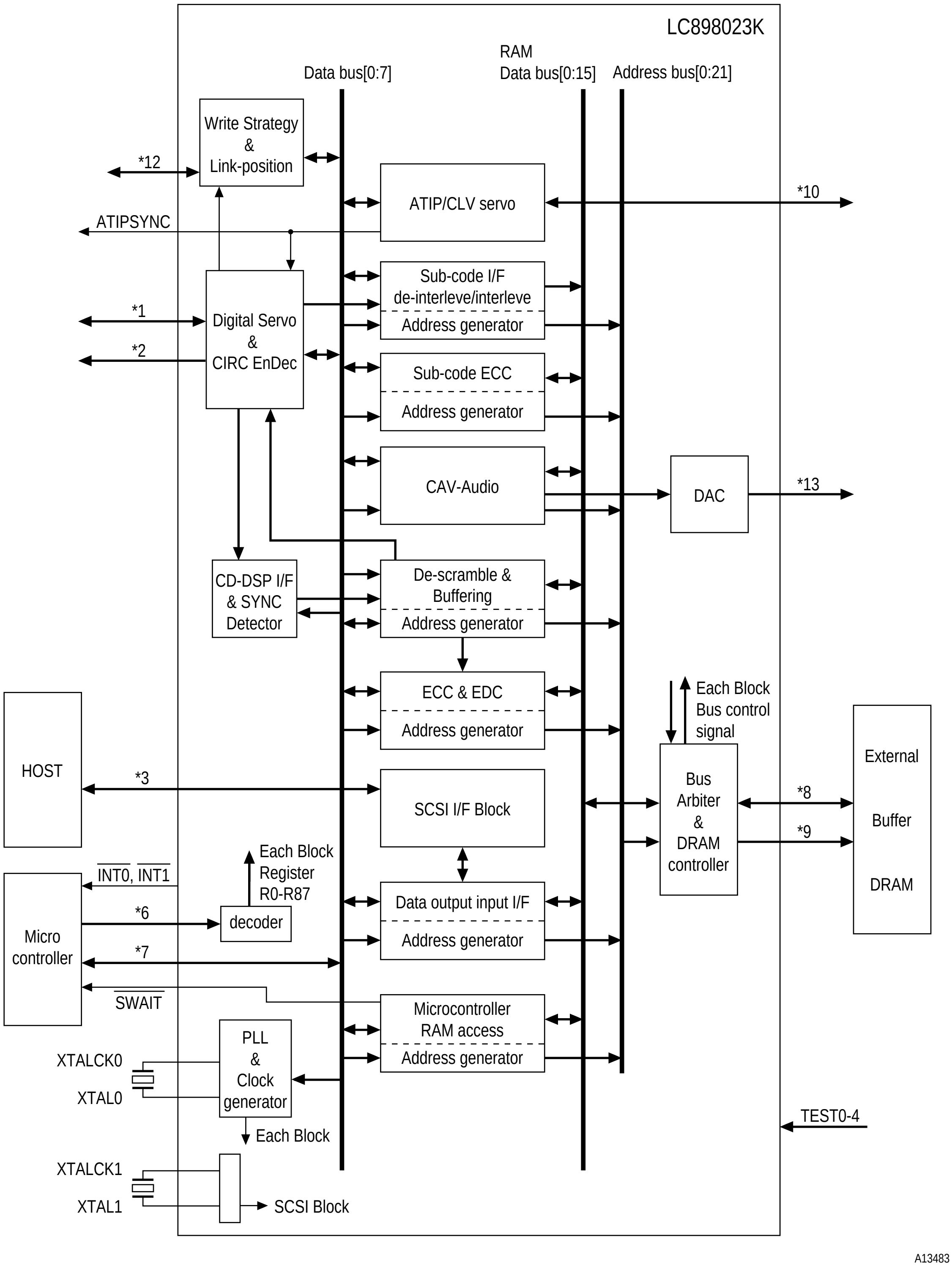
Block Diagram



*1	DSLB (pin96) to FR (pin123), CSS (pin126) to SPDO (pin142), SHOCK (pin147) to PCK2 (pin155)
*2	SUBSYNC
*3	$\overline{\text{DB0}}$ to $\overline{\text{DB7}}$, $\overline{\text{DBP}}$, $\overline{\text{BSY}}$, $\overline{\text{MSG}}$, $\overline{\text{SEL}}$, $\overline{\text{RST}}$, $\overline{\text{REQ}}$, I/O, C/D, $\overline{\text{ACK}}$, $\overline{\text{ATN}}$
*6	$\overline{\text{RD}}$, $\overline{\text{WR}}$, SUA0 to SUA7, $\overline{\text{CS}}$
*7	D0 to D7
*8	IO0 to IO15
*9	RA0 to RA9, $\overline{\text{RAS0}}$, $\overline{\text{RAS1}}$, $\overline{\text{RAS2}}$, $\overline{\text{CAS0}}$, $\overline{\text{CAS1}}$, $\overline{\text{OE}}$, $\overline{\text{UWE}}$, $\overline{\text{LWE}}$
*10	WOBBLE, BIDATA, BICLK, ATIPSYNC
*12	WRITE, SSP2/1, RAPC, WAPC, H11T0, LDH, TEST2/1, WDAT, NWDAT, EFMG
*13	LOUT, ROUT

Pin Functions

Pin type					
I	Input	B	Bidirectional pin	NC	Not connected
O	Output	P	Power supply	A	Analog pin

Pin No.	Pin name	Type	Pin function
1	V_{SS}	P	Digital system ground (V_{SS})
2	RA4	O	CD-ROM encoder/decoder DRAM address lines
3	RA5	O	
4	RA6	O	
5	RA7	O	
6	RA8	O	
7	RA9	O	
8	V_{DD}	P	Digital system power supply (5 V)
9	V_{SS}	P	Digital system ground (V_{SS})
10	IO0	B	CD-ROM encoder/decoder buffer RAM data lines These pins have built-in pull-up resistors.
11	IO1	B	
12	IO2	B	
13	IO3	B	
14	IO4	B	
15	IO5	B	
16	V_{DD}	P	Digital system power supply (3.3 V)
17	V_{SS}	P	Digital system ground (V_{SS})
18	IO6	B	CD-ROM encoder/decoder buffer RAM data lines These pins have built-in pull-up resistors.
19	IO7	B	
20	IO8	B	
21	IO9	B	
22	IO10	B	
23	V_{SS}	P	Digital system ground (V_{SS})
24	V_{DD}	P	Digital system power supply (3.3 V)
25	IO11	B	CD-ROM encoder/decoder buffer RAM data lines
26	IO12	B	
27	IO13	B	
28	IO14	B	
29	IO15	B	
30	ATIPSYNC	I	ATIP SYNC detection signal
31	BIDATA	B	ATIP demodulator I/O signals
32	BICLK	B	
33	WOBBLE	I	
34	V_{DD}	P	Digital system power supply (5 V)
35	V_{SS}	P	Digital system ground (V_{SS})
36	ACRCNG	O	ATIP CRC error signal
37	WRITE	I	Write strategy signal control input
38	SSP2	O	Servo sampling pulse output
39	SSP1	O	Servo sampling pulse output
40	RAPC	O	Laser control sampling pulse output
41	WAPC	O	Laser control sampling pulse output
42	H11T0	O	Running OPC sampling pulse
43	LDH	O	Recording laser diode control signal output
44	V_{DD}	P	Digital system power supply (3.3 V)
45	V_{SS}	P	Digital system ground (V_{SS})
46	ATEST3	O	Analog block test output
47	ATEST1	O	Analog block test output
48	WDAT	O	Recording laser diode control signal output
49	NWDAT	O	Recording laser diode control signal output (WDAT inverted)
50	V_{DD}	P	Analog system power supply (3.3 V)
51	V_{SS}	P	Analog system ground (V_{SS})

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Pin No.	Pin name	Type	Pin function
52	V_{DD}	P	Digital system power supply (5 V)
53	V_{SS}	P	Digital system ground (V_{SS})
54	R1	I	Write strategy analog signals
55	VCNT1	I	
56	MDC1	I	
57	PD1	O	
58	$\overline{\text{SWAIT}}$	O	Wait signal to the microcontroller
59	$\overline{\text{INT0}}$	O	Interrupt request signal outputs to the microcontroller These are open-drain outputs with built-in pull-up resistors.
60	$\overline{\text{INT1}}$	O	
61	D0	B	Microcontroller data signal lines These pins have built-in pull-up resistors.
62	D1	B	
63	D2	B	
64	D3	B	
65	D4	B	
66	D5	B	
67	D6	B	
68	V_{DD}	P	Digital system power supply (5 V)
69	V_{SS}	P	Digital system ground (V_{SS})
70	D7	B	Microcontroller data signal line
71	SUA0	I	Command register selection address
72	SUA1	I	
73	SUA2	I	
74	SUA3	I	
75	SUA4	I	
76	SUA5	I	
77	SUA6	I	
78	SUA7	I	
79	$\overline{\text{CS}}$	I	Chip select signal input from the microcontroller
80	$\overline{\text{RD}}$	I	Data read signal from the microcontroller
81	$\overline{\text{WR}}$	I	Data write signal from the microcontroller
82	TEST0	I	Test pin. This pin must be tied to V_{SS}.
83	VCNT	I	VCO control voltage
84	R	I	VCO bias resistor connection
85	PD	O	Charge pump output
86	V_{DD}	P	Analog system power supply (3.3 V)
87	V_{SS}	P	Analog system ground (V_{SS})
88	TEST1	I	Test pin. This pin must be tied to V_{SS}.
89	$\overline{\text{RESET}}$	I	Reset input
90	XTALCK0	I	Crystal oscillator circuit input (33.8688 MHz)
91	XTAL0	O	Crystal oscillator circuit output
92	ROUT	O	D/A converter output
93	V_{SS}	P	Analog system ground (V_{SS})
94	V_{DD}	P	Analog system power supply (5 V)
95	LOUT	O	D/A converter output
96	DSLB	O	SLC PWM output
97	SLCIST1	I	EFM slice level setting input
98	SLCIST2	I	
99	V_{SS}	P	Analog system ground (V_{SS})
100	V_{DD}	P	Analog system power supply (3.3 V)
101	SLCO0	O	EFM slice level output
102	SLCO1	O	
103	SLCO2	O	
104	V_{DD}	P	Digital system power supply (5 V)
105	V_{SS}	P	Digital system ground (V_{SS})

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Pin No.	Pin name	Type	Pin function
106	SLCO3	O	EFM slice level output
107	EFMIN	I	EFM input
108	EFMIN2	I	
109	TEST4	I	Test pin. This pin must be tied to V_{SS}.
110	JITC	O	Jitter output
111	RPO	O	P/N balance adjustment
112	OPP	I	
113	PCKISTF	I	Frequency comparator charge pump
114	PCKISTP	I	Phase comparator charge pump
115	V_{SS}	P	Analog system ground (V_{SS})
116	V_{DD}	P	Analog system power supply (3.3 V)
117	PDO	O	Charge pump filter
118	PDS1	O	Charge pump selection
119	PDS2	O	
120	V_{DD}	P	Digital system power supply (3.3 V)
121	V_{SS}	P	Digital system ground (V_{SS})
122	PDS3	O	Charge pump selection
123	FR	I	VCO frequency setting
124	TEST2	I	Test pin. This pin must be tied to V_{SS}.
125	TEST3	I	DRAM voltage (5 V/3.3 V) selection pin
126	CSS	I	Center servo input pin
127	AD0	I	AD input
128	RREC	I	Optical signal discrimination input
129	FE	I	FE input
130	TE	I	TE input
131	VREF	I	VREF input
132	AD1	I	AD input
133	V_{SS}	P	Analog system ground (V_{SS})
134	DA0	O	DA output
135	DA1	O	DA output
136	DA2	O	DA output
137	TDO	O	Tracking output
138	V_{DD}	P	Analog system power supply (5 V)
139	V_{SS}	P	Analog system ground (V_{SS})
140	FDO	O	Focus output
141	SLDO	O	Sled output
142	SPDO	O	Spindle output
143	V_{SS}	P	Digital system ground (V_{SS})
144	V_{DD}	P	Digital system power supply (3.3 V)
145	SUBSYNC	O	Subcode SYNC signal
146	EFMG	O	EFM gate signal
147	SHOCK	O	Shock detection signal output
148	LOCK	O	PLL lock state output
149	DEF	I	Defect detection signal input
150	HFL	I	Mirror detection signal input
151	TES	I	TES comparator input
152	EFMO	O	Post-binarization EFM signal output
153	LDON	O	Laser control
154	FG	I	FG input
155	PCK2	O	PCK output
156	V_{DD}	P	Digital system power supply (5 V)
157	V_{SS}	P	Digital system ground (V_{SS})
158	XTALCK1	I	SCSI interface crystal oscillator circuit input (20 MHz)
159	XTAL1	O	SCSI interface crystal oscillator circuit output
160	$\overline{\text{DB0}}$	B	SCSI connection

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Pin No.	Pin name	Type	Pin function
161	V_{SS}	P	Digital system ground (V_{SS})
162	$\overline{\text{DB1}}$	B	SCSI connection
163	$\overline{\text{DB2}}$	B	
164	V_{DD}	P	Digital system power supply (5 V)
165	$\overline{\text{DB3}}$	B	SCSI connection
166	$\overline{\text{DB4}}$	B	
167	V_{SS}	P	Digital system ground (V_{SS})
168	$\overline{\text{DB5}}$	B	SCSI connection
169	$\overline{\text{DB6}}$	B	
170	$\overline{\text{DB7}}$	B	
171	V_{SS}	P	Digital system ground (V_{SS})
172	V_{DD}	P	Digital system power supply (5 V)
173	V_{SS}	P	Digital system ground (V_{SS})
174	$\overline{\text{DBP}}$	B	SCSI connection
175	$\overline{\text{ATN}}$	B	
176	$\overline{\text{BSY}}$	B	
177	V_{SS}	P	Digital system ground (V_{SS})
178	$\overline{\text{ACK}}$	B	SCSI connection
179	$\overline{\text{RST}}$	B	
180	V_{DD}	P	Digital system power supply (5 V)
181	$\overline{\text{MSG}}$	B	SCSI connection
182	$\overline{\text{SEL}}$	B	
183	V_{SS}	P	Digital system ground (V_{SS})
184	C/D	B	SCSI connection
185	V_{SS}	P	Digital system ground (V_{SS})
186	V_{DD}	P	Digital system power supply (5 V)
187	$\overline{\text{REQ}}$	B	SCSI connections
188	I/O	B	
189	V_{SS}	P	Digital system ground (V_{SS})
190	V_{DD}	P	Digital system power supply (3.3 V)
191	V_{SS}	P	Digital system ground (V_{SS})
192		NC	Unused
193		NC	Unused
194	$\overline{\text{RAS0}}$	O	DRAM $\overline{\text{RAS}}$ signal outputs
195	$\overline{\text{RAS1}}$	O	
196	$\overline{\text{RAS2}}$	O	
197	$\overline{\text{LWE}}$	O	DRAM lower write enable
198	V_{DD}	P	Digital system power supply (3.3 V)
199	V_{SS}	P	Digital system ground (V_{SS})
200	$\overline{\text{UWE}}$	O	DRAM upper write enable
201	$\overline{\text{CAS0}}$	O	DRAM $\overline{\text{CAS}}$ signal output
202	$\overline{\text{CAS1}}$	O	
203	$\overline{\text{OE}}$	O	DRAM output enable
204	RA0	O	CD-ROM encoder/decoder DRAM address lines
205	RA1	O	
206	RA2	O	
207	RA3	O	
208	V_{DD}	P	Digital system power supply (3.3 V)

Pin Functions

<SCSI Interface Pins>

$\overline{\text{BSY}}$, $\overline{\text{ACK}}$, $\overline{\text{MSG}}$, $\overline{\text{SEL}}$, $\overline{\text{REQ}}$, $\overline{\text{ATN}}$, $\overline{\text{RST}}$, I/O, C/D (input/output)

SCIS bus control.

$\overline{\text{DB0}}$ to $\overline{\text{DB7}}$, $\overline{\text{DBP}}$ (input/output)

SCSI data bus.

<Microcontroller Interface Pins>

$\overline{\text{CS}}$ (input)

Chip select signal from the microcontroller. The microcontroller interface is active when this pin is low.

$\overline{\text{RD}}$, $\overline{\text{WR}}$ (input)

Connect the microcontroller read and write lines to these inputs.

$\overline{\text{SWAIT}}$ (input)

Wait signal output to the microcontroller. When accessing buffer RAM, the microcontroller must wait if this pin is low.

SUA0 to SUA7 (input)

Internal register address lines

D0 to D7 (input)

Microcontroller data bus. These pins have built-in pull-up resistors.

$\overline{\text{INT0}}$, $\overline{\text{INT1}}$ (output)

Interrupt request signals output to the microcontroller. $\overline{\text{INT1}}$ can be set to output the ATAPI interrupt by setting INT1EN (Conf-R11 bit 7)

These are open drain outputs with built-in 80 kΩ (at room temperature, 5 V) pull-up resistors.

<Buffer RAM Pins>

I/O0 to I/O15 (input/output)

Buffer RAM data bus. These pins have built-in pull-up resistors.

RA0 to RA9 (output)

Buffer RAM address lines.

$\overline{\text{RAS0}}$, $\overline{\text{RAS1}}$, $\overline{\text{RAS2}}$ (output)

Buffer DRAM RAS outputs. Normally, $\overline{\text{RAS0}}$ is used. However, if two 16-Mbit DRAMs are used, connect the $\overline{\text{RAS0}}$ and $\overline{\text{RAS1}}$ lines to the RAS pins on the DRAMs. If four 16-Mbit DRAMs are used, connect the $\overline{\text{RAS0}}$, $\overline{\text{RAS1}}$, $\overline{\text{RAS2}}$, and $\overline{\text{LWE}}$ lines to the RAS pins on the DRAMs.

$\overline{\text{CAS0}}$, $\overline{\text{CAS1}}$ (output)

Buffer DRAM CAS outputs. Normally, $\overline{\text{CAS0}}$ is used. However, if two 16-Mbit DRAMs are used, connect the $\overline{\text{CAS0}}$ output to the CAS pins on the DRAMs. If 2-CAS type DRAMs are used, connect CAS0 to UCAS and CAS1 to LCAS.

$\overline{\text{OE}}$ (output)

Buffer RAM read output.

$\overline{\text{UWE}}$, $\overline{\text{LWE}}$ (output)

Buffer RAM write outputs. Connect these to the corresponding pins. If 2-CAS type DRAMs are used, UWE must be connected. (Leave LWE open.)

1. Analog Interface Pins

CCS (input)

Midpoint servo input pin.

RREC (input)

Optical discrimination input.

FE (input)

Focus error signal input.

TE (input)

Tracking error signal input.

VREF (input)

Input for the servo system reference voltage.

AD0, AD1, AD2 (input)

A/D converter auxiliary inputs.

DA0, DA1, DA2 (input)

D/A converter auxiliary inputs.

TES (input)

TES comparator input.

TDO (output)

Tracking control signal output.

FDO (output)

Focus control signal output.

SLDO (output)

Sled control signal output.

SPDO (output)

Spindle control signal output.

2. EFM Input Block Pins

EFMIN (input)

EFM signal input.

The high-frequency components of the RF signal acquired from the RF amplifier are cut with a capacitor, and this pin inputs that signal biased by the value of the SLCO0 to SLCO3 outputs passed through a low-pass filter.

EFMIN2 (input)

Used to change the time constant of the low-pass filter.

SLCIST1, SLCIST2 (input)

Slice level controller charge pump bias resistor connection.

SLCO0, SLCO1, SLCO2, SLCO3 (output)

Slice level controller charge pump outputs.

These levels bias the RF signal input to the EFMIN pin after being passed through a low-pass filter.

DSLB (output)

Slice level control PWM output.

EFMO (output)

Post-binarization EFM signal output. (For monitoring)

3. EFM Clock Generation Block Pins

FR (input)

EFM reproduction PLL VCO bias resistor connection.

PDO, PDS1, PDS2, PDS3 (output)

EFM reproduction PLL lag-lead filter connection.

PCKISTF (input)

EFM reproduction PLL frequency comparator charge pump bias resistor connection.

PCKISTP (input)

EFM reproduction PLL phase comparator charge pump bias resistor connection.

RPO (output)

P/N balance adjustment.

OPP (input)

P/N balance adjustment.

PCK2 (output)

EFM reproduction bit clock output.

4. Jitter Discrimination Pins

JITC (output)

Jitter output.

5. Spindle Speed Detection Pins

FG (input)

Input for the speed monitor signal from the spindle driver.

6. Audio Interface Pins

LOUT, ROUT (output)

Left and right channel audio signal outputs.

7. RF Amplifier Interface Pins

LDON (output)

RF amplifier interface.

8. Write Strategy Pins

WRITE, SSP2/1, RAPC, WAPC, H11T0, LDH, ATEST3, 1, WDAT, NWDAT (I/O)

Write strategy signal connections.

9. ATIP Decoder Related Pins

ATIPSYNC (output)

ATIP synchronization detection signal. (For monitoring)

BIDATA, BICLK (I/O)

Input mode: Input of the biphase data and biphase clock when an external ATIP demodulator is used.

Output mode: Output of the biphase data and biphase clock when the internal ATIP demodulator is used. (For monitoring)

WOBBLE (input)

Wobble signal is input when the internal ATIP demodulator is used.

ACRCNG (output)

Outputs the result of the ATIP decoder CRC check. (For monitoring)

<Other Pins>

$\overline{\text{RESET}}$ (input)

The LC898023K reset input. A low level input resets the LC898023K.

This pin must be held low for at least 1 µs when power is first applied.

TEST4 to TEST0 (input)

Test inputs. These pins must be connected to ground.

XTALCK0 (input), **XTAL0** (output)

Drive these pins at 33.8688 MHz. This signal is used, without modification, as main clock for the CD-ROM encoder and decoder blocks, including the DRAM interface.

XTALCK1 (input), **XTAL1** (output)

Main clock for the SCSI block. The LC898023K is designed so that it can operate even when the ECC and SCSI blocks are not synchronized. Providing a 20 MHz input to the XTALCK0 and XTALCK1 pins assures that correct, synchronized transfer at 10 Mbyte/s (20 Mbyte/s for Ultra SCSI) can be achieved. The maximum frequency that can be used is 20 MHz.

Since both edges of the clock signal are used by Ultra SCSI, the duty ratio must be correct. Add feedback resistors on the XTALCK1 and XTAL1 pins and take other measures as required.

R, VCNT, PDO, R1, VCNT1, PD1, MDC1 (I/O)

Clock reproduction PLL circuit pins.

SUBSYNC (output)

Subcode SYNC output signal from the CIRC encoder during recording. (For monitoring)

EFMG (output)

Outputs a high level during recording.

SHOCK (output)

Outputs a high level when a mechanical shock is detected.

LOCK (output)

Outputs a high level when the PLL circuit is locked.

DEF (input)

Inputs the defect detection signal.

HFL (input)

Inputs the mirror detection signal.

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