PRELIMINARY PRODUCT INFORMATION

NEC

MOS INTEGRATED CIRCUIT

μPD784217Y,784218Y

16/8-BIT SINGLE-CHIP MICROCONTROLLERS

The μPD784218Y is based on the μPD784218 with an I^2C bus control function appended, and is ideal for applications in audio-visual.

A flash memory version, the μPD78F4218Y, which can operate in the same supply voltage range as the mask ROM version, and various development tools are under development.

The functions are explained in detail in the following user's manuals. Be sure to read these manuals when designing your system.

μPD784218, 784218Y Subseries User's Manual	**Hardware**	**: Planned**
78K/IV Series User's Manual	**Instructions**	**: U10905E**

FEATURES

- On-chip I^2C bus
- ROM correction function
- Inherits peripheral functions of μPD78078Y Subseries
- Pin-compatible with μPD784218 Subseries
- Minimum instruction execution time
  160 ns (main system clock f_{XX} = 12.5 MHz)
  61 μs (subsystem clock f_{XT} = 32.768 kHz)
- High-capacity memory
- ROM: 192 Kbytes (μPD784217Y)
  256 Kbytes (μPD784218Y)
- RAM: 12 800 bytes (μPD784217Y, 784218Y)
- I/O port: 86 pins
- Timer/counter: 16-bit timer/counter × 1 unit
  8-bit timer/counter × 6 units
- Serial interface: 3 channels
  UART/IOE (3-wire serial I/O): 2 channels
  CSI (3-wire serial I/O, multi-master supporting I^2C bus): 1 channel
- Standby function
  HALT/STOP/IDLE mode
  In power-saving mode: HALT/IDLE mode (with subsystem clock)
- Clock division function
- Watch timer: 1 channel
- Watchdog timer: 1 channel
- Clock output function
  f_{XX}, $f_{XX}/2$, $f_{XX}/2^2$, $f_{XX}/2^3$, $f_{XX}/2^4$, $f_{XX}/2^5$, $f_{XX}/2^6$, $f_{XX}/2^7$, f_{XT} selectable
- Buzzer output function
  $f_{XX}/2^{10}$, $f_{XX}/2^{11}$, $f_{XX}/2^{12}$, $f_{XX}/2^{13}$ selectable
- A/D converter: 8-bit resolution × 8 channels
- D/A converter: 8-bit resolution × 2 channels
- Supply voltage: V_{DD} = 1.8 to 5.5 V

APPLICATION FIELDS

Cellular telephones, PHS, cordless telephones, CD-ROM, AV systems, etc.

Unless mentioned otherwise, references in this document to the μPD784218Y refer to the μPD784217Y and μPD784218Y.

The information contained in this document is being issued in advance of the production cycle for the device. The parameters for the device may change before final production or NEC Corporation, at its own discretion, may withdraw the device prior to its production.

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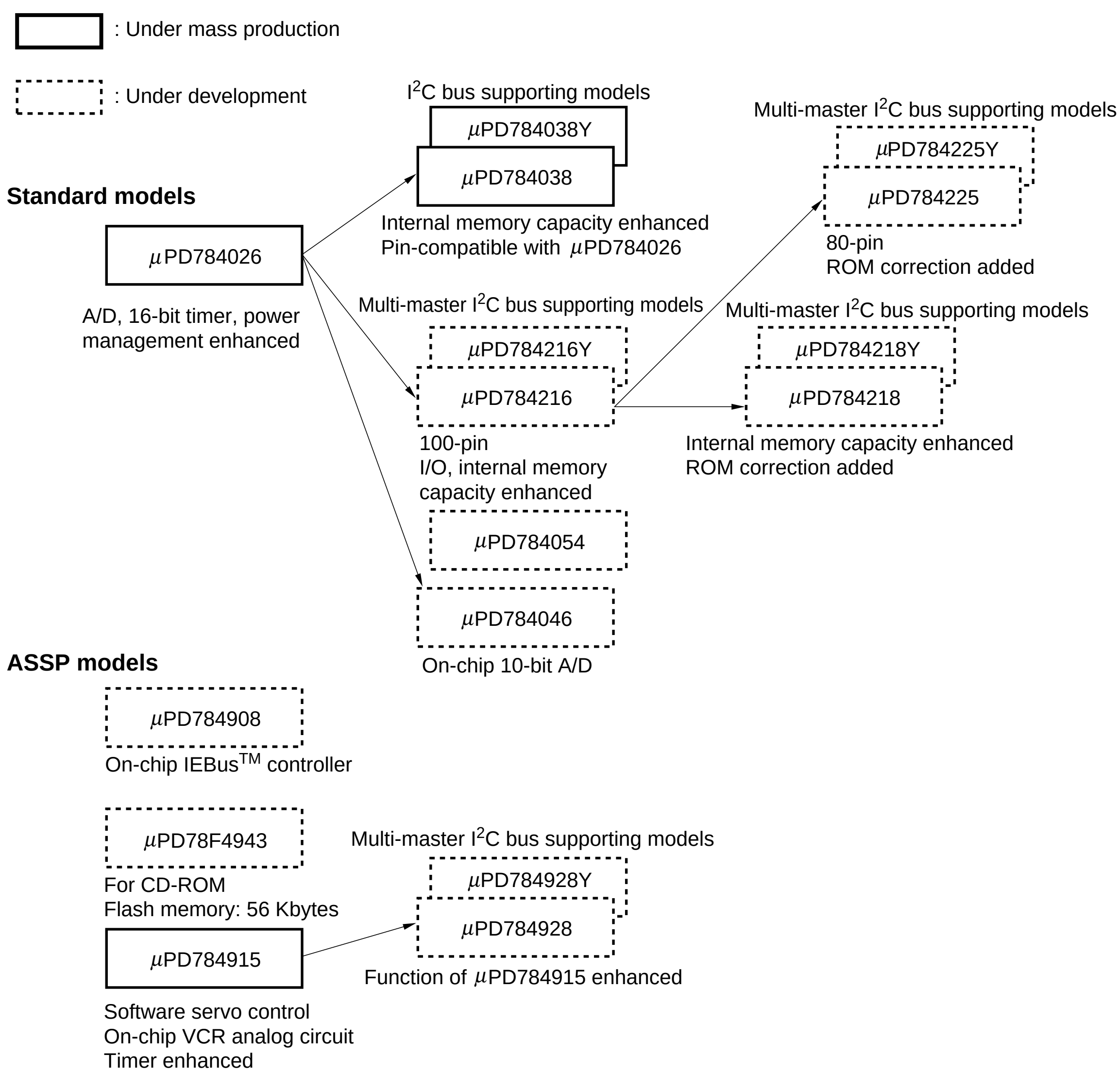
ORDERING INFORMATION

Part Number	Package	Internal ROM (Bytes)	Internal RAM (Bytes)
μPD784217YGC-×××-7EA	100-pin plastic QFP (fine pitch) (14 × 14 mm)	192 K	12 800
μPD784217YGF-×××-3BA	100-pin plastic QFP (14 × 20 mm)	192 K	12 800
μPD784218YGC-×××-7EA	100-pin plastic QFP (fine pitch) (14 × 14 mm)	256 K	12 800
μPD784218YGF-×××-3BA	100-pin plastic QFP (14 × 20 mm)	256 K	12 800

Remark ××× indicates a ROM code suffix.

78K/IV Series Product Development



FUNCTIONS (1/2)

Item \ Part Number			μPD784217Y	μPD784218Y
Number of basic instructions (mnemonics)			113	
General-purpose register			8 bits × 16 registers × 8 banks, or 16 bits × 8 registers × 8 banks (memory mapping)	
Minimum instruction execution time			• 160 ns/320 ns/640 ns/1 280 ns/2 560 ns (main system clock: f_{XX} = 12.5 MHz) • 61 μs (subsystem clock: f_{XT} = 32.768 kHz)	
Internal memory		ROM	192 Kbytes	256 Kbytes
		RAM	12 800 bytes	
Memory space			1 Mbyte with program and data spaces combined	
I/O port		Total	86	
		CMOS input	8	
		CMOS I/O	72	
		N-ch open-drain I/O	6	
	Pins with ancillary functions[Note]	Pins with pull-up resistor	70	
		LED direct drive output	22	
		Medium-voltage pin	6	
Real-time output port			4 bits × 2, or 8 bits × 1	
Timer/counter			16-bit timer/counter : Timer register × 1, Capture/compare register × 2; Pulse output • PWM/PPG output • Square wave output • One-shot pulse output	
			8-bit timer/counter 1 : Timer register × 1, Compare register × 1; Pulse output • PWM output • Square wave output	
			8-bit timer/counter 2 : Timer register × 1, Compare register × 1; Pulse output • PWM output • Square wave output	
			8-bit timer/counter 5 : Timer register × 1, Compare register × 1; Pulse output • PWM output • Square wave output	
			8-bit timer/counter 6 : Timer register × 1, Compare register × 1; Pulse output • PWM output • Square wave output	
			8-bit timer/counter 7 : Timer register × 1, Compare register × 1; Pulse output • PWM output • Square wave output	
			8-bit timer/counter 8 : Timer register × 1, Compare register × 1; Pulse output • PWM output • Square wave output	

Note The pins with ancillary functions are included in the I/O pins.

FUNCTIONS (2/2)

Item \ Part Number		μPD784217Y	μPD784218Y
Serial interface		UART/IOE (3-wire serial I/O): 2 channels (on-chip baud rate generator) CSI (3-wire serial I/O, I^2C bus supporting multi-master): 1 channel	
A/D converter		8-bit resolution × 8 channels	
D/A converter		8-bit resolution × 2 channels	
Clock output		Selectable from f_{XX}, $f_{XX}/2$, $f_{XX}/2^2$, $f_{XX}/2^3$, $f_{XX}/2^4$, $f_{XX}/2^5$, $f_{XX}/2^6$, $f_{XX}/2^7$, f_{XT}	
Buzzer output		Selectable from $f_{XX}/2^{10}$, $f_{XX}/2^{11}$, $f_{XX}/2^{12}$, $f_{XX}/2^{13}$	
Watch timer		1 channel	
Watchdog timer		1 channel	
Standby		• HALT/STOP/IDLE mode • In power-saving mode (with subsystem clock): HALT/IDLE mode	
Interrupt	Hardware	29 (internal: 20, external: 9)	
	Software	BRK instruction, BRKCS instruction, operand error	
	Non-maskable	Internal: 1, external: 1	
	Maskable	Internal: 19, external: 8	
		• 4 programmable priority levels • 3 service modes: vectored interrupt/macro service/context switching	
Supply voltage		V_{DD} = 1.8 to 5.5 V	
Package		100-pin plastic QFP (fine pitch) (14 × 14 mm) 100-pin plastic QFP (14 × 20 mm)	

CONTENTS

1. DIFFERENCES AMONG MODELS IN μPD784218Y SUBSERIES

The only difference among the μPD784217Y and 784218Y lies in the internal memory capacity.

The μPD78F4218Y is provided with a 256-Kbyte flash memory instead of the mask ROM of the μPD784218Y. These differences are summarized in Table 1-1.

Table 1-1. Differences among Models in μPD784218Y Subseries

Item \ Part Number	μPD784217Y	μPD784218Y	μPD78F4218Y
Internal ROM	192 Kbytes (mask ROM)	256 Kbytes (mask ROM)	256 Kbytes (Flash memory)
Internal RAM	12 800 bytes		
Internal memory size switching register (IMS)	None		Provided
V_{PP} pin	None		Provided

2. DIFFERENCES BETWEEN μPD784218Y AND μPD784216Y

The differences between the μPD784218Y and 784216Y are summarized in Table 2-1.

Table 2-1. Differences between μPD784218Y and μPD784216Y

Item \ Part Number	μPD784218Y	μPD784216Y
Internal ROM	256 Kbytes	128 Kbytes
Internal RAM	12 800 bytes	8 192 bytes
ROM correction	Provided	None
External access status function	Provided	None

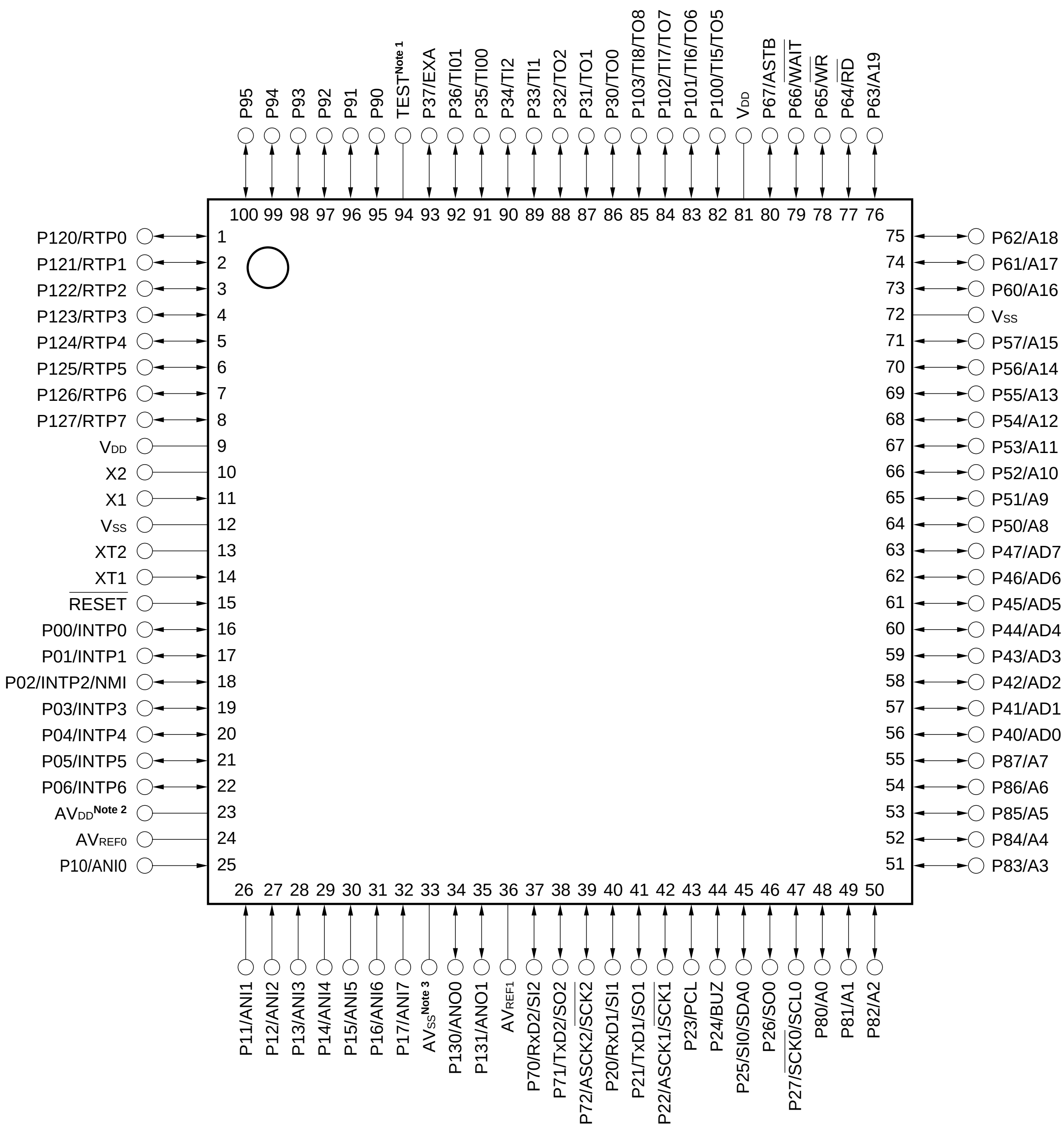
3. MAIN DIFFERENCES FROM μPD78078Y SUBSERIES

Item		Series Name: μPD784218Y Subseries	μPD78078Y Subseries
CPU		16-bit CPU	8-bit CPU
Minimum instruction execution time	With main system clock	160 ns (at 12.5 MHz)	400 ns (at 5.0 MHz)
	With subsystem clock	61 μs (at 32.768 kHz)	122 μs (at 32.768 kHz)
Memory space		1 Mbyte	64 Kbytes
I/O port	Total	86	88
	CMOS input	8	2
	CMOS I/O	72	78
	N-ch open-drain I/O	6	8
Pins with ancillary functions Note	Pins with pull-up resistor	70	86
	LED direct drive output	22	16
	Medium-voltage pin	6	8
Timer/counter		• 16-bit timer/counter × 1 unit • 8-bit timer/counter × 6 units	• 16-bit timer/counter × 1 unit • 8-bit timer/counter × 4 units
Serial interface		• UART/IOE (3-wire serial I/O) × 2 channels • CSI (3-wire serial I/O, multi-master supporting I^2C bus) × 1 channel	• UART/IOE (3-wire serial I/O) × 1 channel • CSI (3-wire serial I/O, 2-wire serial I/O, I^2C bus) × 1 channel • CSI (3-wire serial I/O, 3-wire serial I/O with automatic transmit/receive function) × 1 channel
Interrupt	NMI pin	Provided	None
	Macro service	Provided	None
	Context switching	Provided	None
	Programmable priority	4 levels	None
Standby function		• HALT/STOP/IDLE mode • In power-saving mode: HALT/IDLE mode	2 modes: HALT/STOP
ROM correction		Provided	None
External access status function		Provided	None
Package		• 100-pin plastic QFP (fine pitch) (14 × 14 mm) • 100-pin plastic QFP (14 × 20 mm)	• 100-pin plastic QFP (fine pitch) (14 × 14 mm) • 100-pin plastic QFP (14 × 20 mm) • 100-pin ceramic WQFN (14 × 20 mm) (μPD78P078Y only)

Note The pins with ancillary functions are included in the I/O pins.

4. PIN CONFIGURATION (Top View)

- **100-pin plastic QFP (fine pitch) (14 × 14 mm)**
  μPD784217YGC-×××-7EA
  μPD784218YGC-×××-7EA

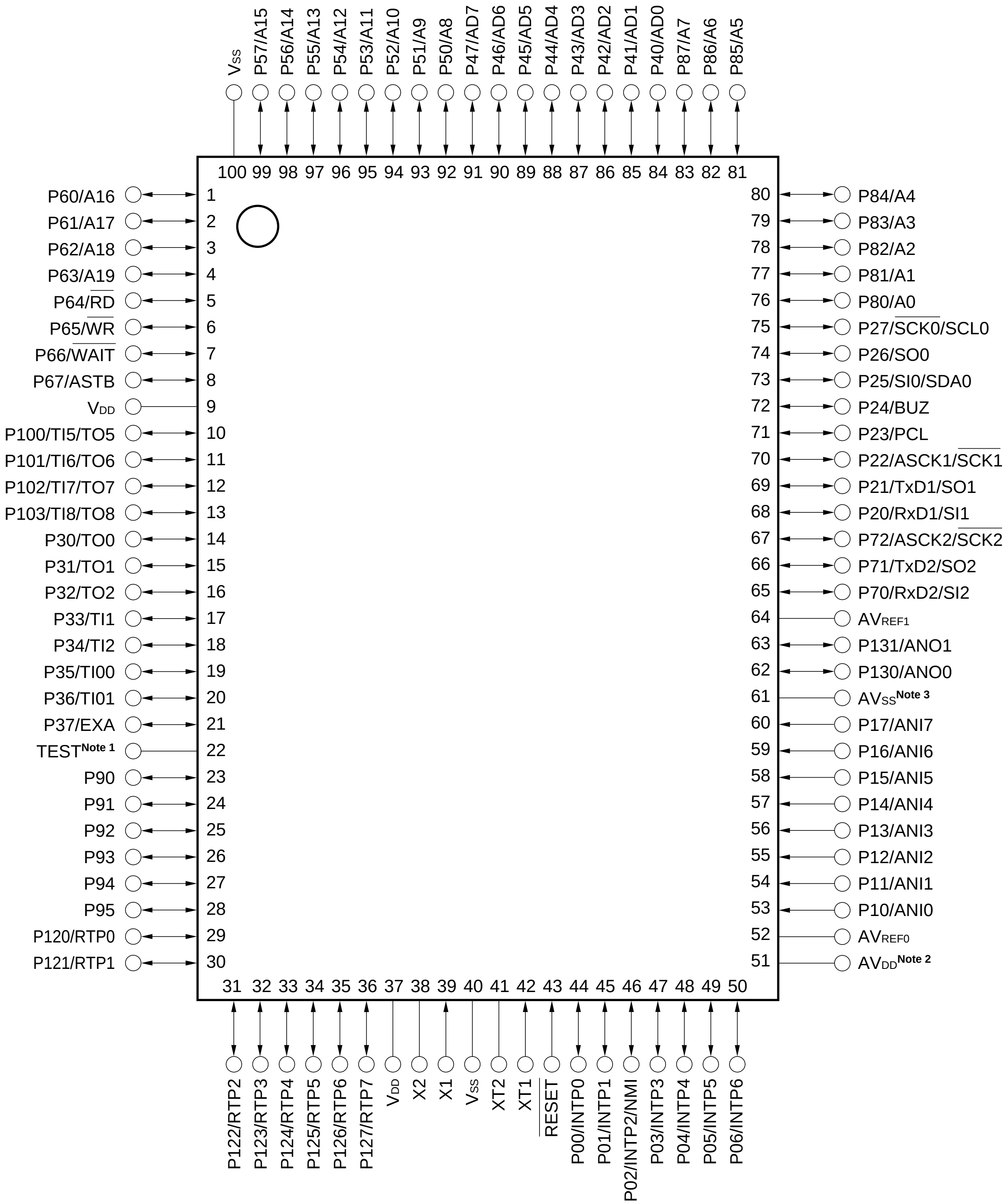


Notes 1. Directly connect the TEST pin to V_{SS}.

2. Connect the AV_{DD} pin to V_{DD}.

3. Connect the AV_{SS} pin to V_{SS}.

- **100-pin plastic QFP (14 × 20 mm)**
  μPD784217YGF-×××-3BA
  μPD784218YGF-×××-3BA



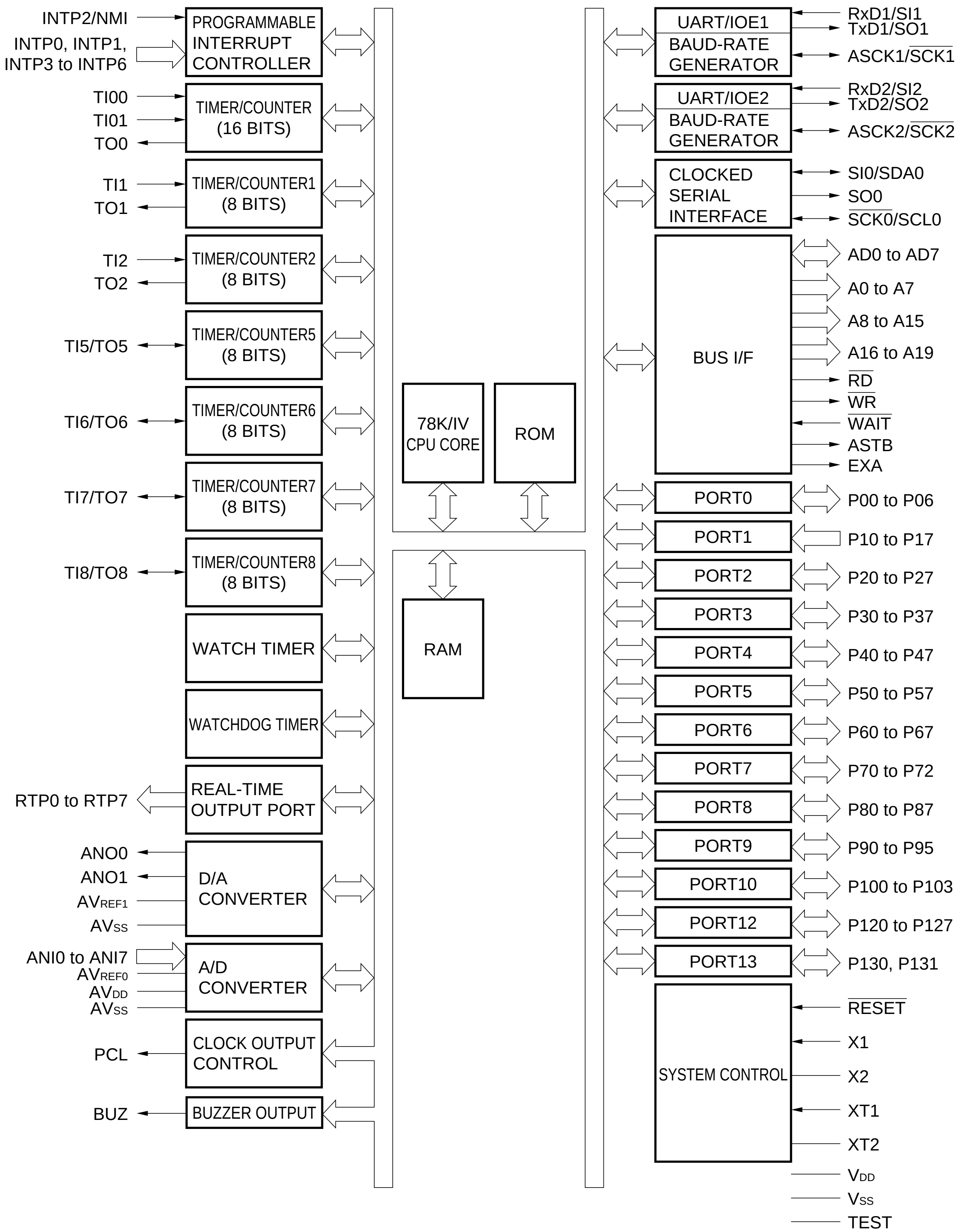
Notes 1. Directly connect the TEST pin to V_{SS}.

2. Connect the AV_{DD} pin to V_{DD}.

3. Connect the AV_{SS} pin to V_{SS}.

A0 to A19	: Address Bus
AD0 to AD7	: Address/Data Bus
ANI0 to ANI7	: Analog Input
ANO0, ANO1	: Analog Output
ASCK1, ASCK2	: Asynchronous Serial Clock
ASTB	: Address Strobe
AV_{DD}	: Analog Power Supply
AV_{REF0}, AV_{REF1}	: Analog Reference Voltage
AV_{SS}	: Analog Ground
BUZ	: Buzzer Clock
EXA	: External Access Status Output
INTP0 to INTP6	: Interrupt from Peripherals
NMI	: Non-maskable Interrupt
P00 to P06	: Port0
P10 to P17	: Port1
P20 to P27	: Port2
P30 to P37	: Port3
P40 to P47	: Port4
P50 to P57	: Port5
P60 to P67	: Port6
P70 to P72	: Port7
P80 to P87	: Port8
P90 to P95	: Port9
P100 to P103	: Port10
P120 to P127	: Port12
P130, P131	: Port13
PCL	: Programmable Clock
$\overline{RD}$	: Read Strobe
$\overline{RESET}$	: Reset
RTP0 to RTP7	: Real-time Output Port
RxD1, RxD2	: Receive Data
$\overline{SCK0}$ to $\overline{SCK2}$	: Serial Clock
SCL0	: Serial Clock
SDA0	: Serial Data
SI0 to SI2	: Serial Input
SO0 to SO2	: Serial Output
TEST	: Test
TI00, TI01, TI1, TI2, TI5 to TI8	: Timer Input
TO0 to TO2, TO5 to TO8	: Timer Output
TxD1, TxD2	: Transmit Data
V_{DD}	: Power Supply
V_{SS}	: Ground
$\overline{WAIT}$	: Wait
$\overline{WR}$	: Write Strobe
X1, X2	: Crystal (Main System Clock)
XT1, XT2	: Crystal (Subsystem Clock)

5. BLOCK DIAGRAM



Remark The internal ROM capacity differs depending on the model.

6. PIN FUNCTION

6.1 Port Pins (1/2)

Pin Name	I/O	Alternate Function	Function
P00	I/O	INTP0	Port 0 (P0): • 7-bit I/O port • Can be set in input or output mode bit-wise. • Pins set in input mode can be connected to internal pull-up resistors by software bit-wise.
P01		INTP1	
P02		INTP2/NMI	
P03		INTP3	
P04		INTP4	
P05		INTP5	
P06		INTP6	
P10 to P17	Input	ANI0 to ANI7	Port 1 (P1): • 8-bit input port
P20	I/O	RxD1/SI1	Port 2 (P2): • 8-bit I/O port • Can be set in input or output mode bit-wise. • Pins set in input mode can be connected to internal pull-up resistors by software bit-wise.
P21		TxD1/SO1	
P22		ASCK1/$\overline{\text{SCK1}}$	
P23		PCL	
P24		BUZ	
P25		SI0/SDA0	
P26		SO0	
P27		$\overline{\text{SCK0}}$/SCL0	
P30	I/O	TO0	Port 3 (P3): • 8-bit I/O port • Can be set in input or output mode bit-wise. • Pins set in input mode can be connected to internal pull-up resistors by software bit-wise.
P31		TO1	
P32		TO2	
P33		TI1	
P34		TI2	
P35		TI00	
P36		TI01	
P37		EXA	
P40 to P47	I/O	AD0 to AD7	Port 4 (P4): • 8-bit I/O port • Can be set in input or output mode bit-wise. • All pins set in input mode can be connected to internal pull-up resistors by software. • Can directly drive LEDs.
P50 to P57	I/O	A8 to A15	Port 5 (P5): • 8-bit I/O port • Can be set in input or output mode bit-wise. • All pins set in input mode can be connected to internal pull-up resistors by software. • Can directly drive LEDs.

6.1 Port Pins (2/2)

Pin Name	I/O	Alternate Function	Function
P60	I/O	A16	Port 6 (P6): • 8-bit I/O port • Can be set in input or output mode bit-wise. • All pins set in input mode can be connected to internal pull-up resistors by software.
P61		A17	
P62		A18	
P63		A19	
P64		$\overline{RD}$	
P65		$\overline{WR}$	
P66		$\overline{WAIT}$	
P67		ASTB	
P70	I/O	RxD2/SI2	Port 7 (P7): • 3-bit I/O port • Can be set in input or output mode bit-wise. • Pins set in input mode can be connected to internal pull-up resistor by software bit-wise.
P71		TxD2/SO2	
P72		ASCK2/$\overline{SCK2}$	
P80 to P87	I/O	A0 to A7	Port 8 (P8): • 8-bit I/O port • Can be set in input or output mode bit-wise. • Pins set in input mode can be connected to internal pull-up resistor by software bit-wise. • Interrupt control flag (KRIF) is set to 1 when falling edge is detected at a pin of this port.
P90 to P95	I/O	—	Port 9 (P9): • N-ch open-drain medium-voltage I/O port • 6-bit I/O port • Can be set in input or output mode bit-wise. • Can directly drive LEDs.
P100	I/O	TI5/TO5	Port 10 (P10): • 4-bit I/O port • Can be set in input or output mode bit-wise. • Pins set in input mode can be connected to internal pull-up resistor by software bit-wise.
P101		TI6/TO6	
P102		TI7/TO7	
P103		TI8/TO8	
P120 to P127	I/O	RTP0 to RTP7	Port 12 (P12): • 8-bit I/O port • Can be set in input or output mode bit-wise. • Pins set in input mode can be connected to internal pull-up resistor by software bit-wise.
P130, P131	I/O	ANO0, ANO1	Port 13 (P13): • 2-bit I/O port • Can be set in input or output mode bit-wise.

6.2 Non-port Pins (1/2)

Pin Name	I/O	Alternate Function	Function
TI00	Input	P35	External count clock input to 16-bit timer register
TI01		P36	Capture trigger signal input to capture/compare register 00
TI1		P33	External count clock input to 8-bit timer register 1
TI2		P34	External count clock input to 8-bit timer register 2
TI5		P100/TO5	External count clock input to 8-bit timer register 5
TI6		P101/TO6	External count clock input to 8-bit timer register 6
TI7		P102/TO7	External count clock input to 8-bit timer register 7
TI8		P103/TO8	External count clock input to 8-bit timer register 8
TO0	Output	P30	16-bit timer output (shared by 14-bit PWM output)
TO1		P31	8-bit timer output (shared by 8-bit PWM output)
TO2		P32	
TO5		P100/TI5	
TO6		P101/TI6	
TO7		P102/TI7	
TO8		P103/TI8	
RxD1	Input	P20/SI1	Serial data input (UART1)
RxD2		P70/SI2	Serial data input (UART2)
TxD1	Output	P21/SO1	Serial data output (UART1)
TxD2		P71/SO2	Serial data output (UART2)
ASCK1	Input	P22/$\overline{\text{SCK1}}$	Baud rate clock input (UART1)
ASCK2		P72/$\overline{\text{SCK2}}$	Baud rate clock input (UART2)
SI0	Input	P25/SDA0	Serial data input (3-wire serial I/O0)
SI1		P20/RxD1	Serial data input (3-wire serial I/O1)
SI2		P70/RxD2	Serial data input (3-wire serial I/O2)
SO0	Output	P26	Serial data output (3-wire serial I/O0)
SO1		P21/TxD1	Serial data output (3-wire serial I/O1)
SO2		P71/TxD2	Serial data output (3-wire serial I/O2)
SDA0	I/O	P25/SI0	Serial data input/output (I^2C bus)
$\overline{\text{SCK0}}$	I/O	P27/SCL0	Serial clock input/output (3-wire serial I/O0)
$\overline{\text{SCK1}}$		P22/ASCK1	Serial clock input/output (3-wire serial I/O1)
$\overline{\text{SCK2}}$		P72/ASCK2	Serial clock input/output (3-wire serial I/O2)
SCL0		P27/$\overline{\text{SCK0}}$	Serial clock input/output (I^2C bus)
NMI	Input	P02/INTP2	Non-maskable interrupt request input
INTP0		P00	External interrupt request input
INTP1		P01	
INTP2		P02/NMI	
INTP3		P03	
INTP4		P04	
INTP5		P05	
INTP6		P06	

6.2 Non-port Pins (2/2)

Pin Name	I/O	Alternate Function	Function
PCL	Output	P23	Clock output (for trimming main system clock and subsystem clock)
BUZ	Output	P24	Buzzer output
RTP0 to RTP7	Output	P120 to P127	Real-time output port that outputs data in synchronization with trigger
AD0 to AD7	I/O	P40 to P47	Low-order address/data bus when external memory is connected
A0 to A7	Output	P80 to P87	Low-order address bus when external memory is connected
A8 to A15		P50 to P57	Middle-order address bus when external memory is connected
A16 to A19		P60 to P63	High-order address bus when external memory is connected
$\overline{RD}$	Output	P64	Strobe signal output for read operation of external memory
$\overline{WR}$		P65	Strobe signal output for write operation of external memory
$\overline{WAIT}$	Input	P66	To insert wait state(s) when external memory is accessed
ASTB	Output	P67	Strobe output to externally latch address information output to ports 4 through 6 and port 8 to access external memory
EXA	Output	P37	Status signal output when external memory is accessed
$\overline{RESET}$	Input	—	System reset input
X1	Input	—	Crystal connection for main system clock oscillation
X2	—		
XT1	Input	—	Crystal connection for subsystem clock oscillation
XT2	—		
ANI0 to ANI7	Input	P10 to P17	Analog voltage input for A/D converter
ANO0, ANO1	Output	P130, P131	Analog voltage output for D/A converter
AV_{REF0}	—	—	To apply reference voltage for A/D converter
AV_{REF1}			To apply reference voltage for D/A converter
AV_{DD}			Positive power supply for A/D converter. Connected to V_{DD}.
AV_{SS}			GND for A/D converter and D/A converter. Connected to V_{SS}.
V_{DD}			Positive power supply
V_{SS}			GND
TEST			Directly connect this pin to V_{SS} (this pin is for IC test).

6.3 Pin I/O Circuits and Recommended Connections of Unused Pins

Table 6-1 shows symbols indicating the I/O circuit types of the respective pins and the recommended connection of unused pins.

For the circuit diagram of each type of I/O circuit, refer to Figure 6-1.

Table 6-1. I/O Circuit Type of Respective Pins and Recommended Connections of Unused Pins (1/2)

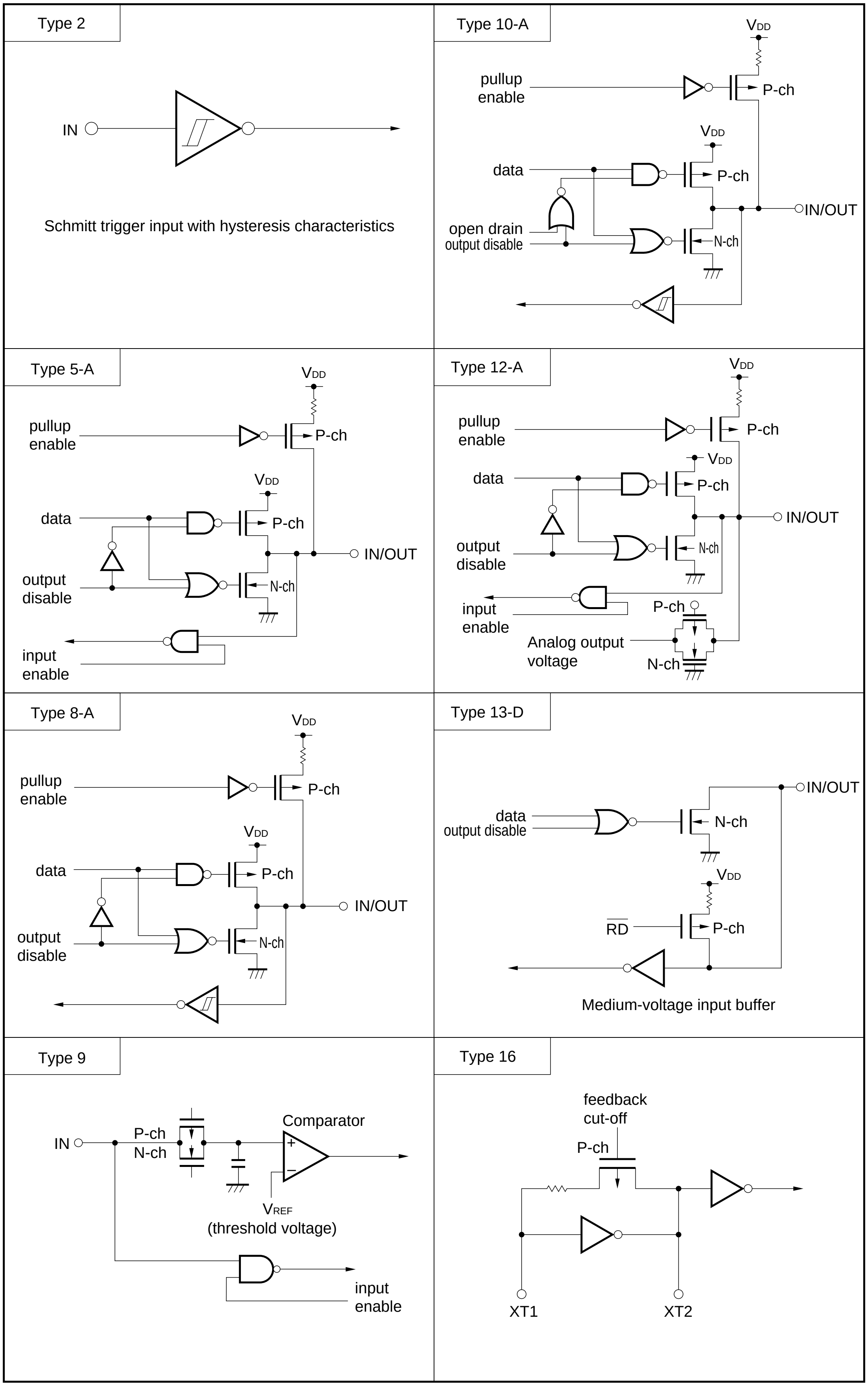
Pin Name	I/O Circuit Type	I/O	Recommended Connections of Unused Pins
P00/INTP0	8-A	I/O	Input : Individually connected to V_{SS} via resistor Output: Open
P01/INTP1			
P02/INTP2/NMI			
P03/INTP3 to P06/INTP6			
P10/ANI0 to P17/ANI7	9	Input	Connected to V_{SS} or V_{DD}
P20/RxD1/SI1	10-A	I/O	Input : Individually connected to V_{SS} via resistor Output: Open
P21/TxD1/SO1			
P22/ASCK1/$\overline{\text{SCK1}}$			
P23/PCL			
P24/BUZ			
P25/SDA0/SI0			
P26/SO0			
P27/SCL0/$\overline{\text{SCK0}}$			
P30/TO0 to P32/TO2	8-A		
P33/TI1, P34/TI2			
P35/TI00, P36/TI01			
P37/EXA			
P40/AD0 to P47/AD7	5-A		
P50/A8 to P57/A15			
P60/A16 to P63/A19			
P64/$\overline{\text{RD}}$			
P65/$\overline{\text{WR}}$			
P66/$\overline{\text{WAIT}}$			
P67/ASTB			
P70/RxD2/SI2	8-A		
P71/TxD2/SO2			
P72/ASCK2/$\overline{\text{SCK2}}$			
P80/A0 to P87/A7			
P90 to P95	13-D		
P100/TI5/TO5	8-A		
P101/TI6/TO6			
P102/TI7/TO7			
P103/TI8/TO8			
P120/RTP0 to P127/RTP7			
P130/ANO0, P131/ANO1	12-A		

Table 6-1. I/O Circuit Type of Respective Pins and Recommended Connections of Unused Pins (2/2)

Pin Name	I/O Circuit Type	I/O	Recommended Connections of Unused Pins
$\overline{RESET}$	2	Input	—
XT1	16		Connected to V_{SS}
XT2		—	Open
AV_{REF0}	—		Connected to V_{SS}
AV_{REF1}			Connected to V_{DD}
AV_{DD}			
AV_{SS}			Connected to V_{SS}
TEST			Directly connected to V_{SS}

Remark Because the circuit type numbers are standardized among the 78K Series products, they are not sequential in some models (i.e., some circuits are not provided).

Figure 6-1. Types of Pin I/O Circuits



7. CPU ARCHITECTURE

7.1 Memory Space

A memory space of 1 Mbyte can be accessed. Mapping of the internal data area (special function registers and internal RAM) can be specified by the LOCATION instruction. The LOCATION instruction must be always executed after reset cancellation, and must not be used more than once.

(1) When LOCATION 0 instruction is executed

- **Internal memory**

  The internal data area and internal ROM area are mapped as follows:

Part Number	Internal Data Area	Internal ROM Area
μPD784217Y	0CD00H to 0FFFFH	00000H to 0CCFFH 10000H to 2FFFFH
μPD784218Y		00000H to 0CCFFH 10000H to 3FFFFH

Caution The following areas that overlap the internal data area of the internal ROM cannot be used when the LOCATION 0 instruction is executed.

Part Number	Unusable Area
μPD784217Y	0CD00H to 0FFFFH (13 056 bytes)
μPD784218Y	

- **External memory**

  The external memory is accessed in external memory expansion mode.

(2) When LOCATION 0FH instruction is executed

- **Internal memory**

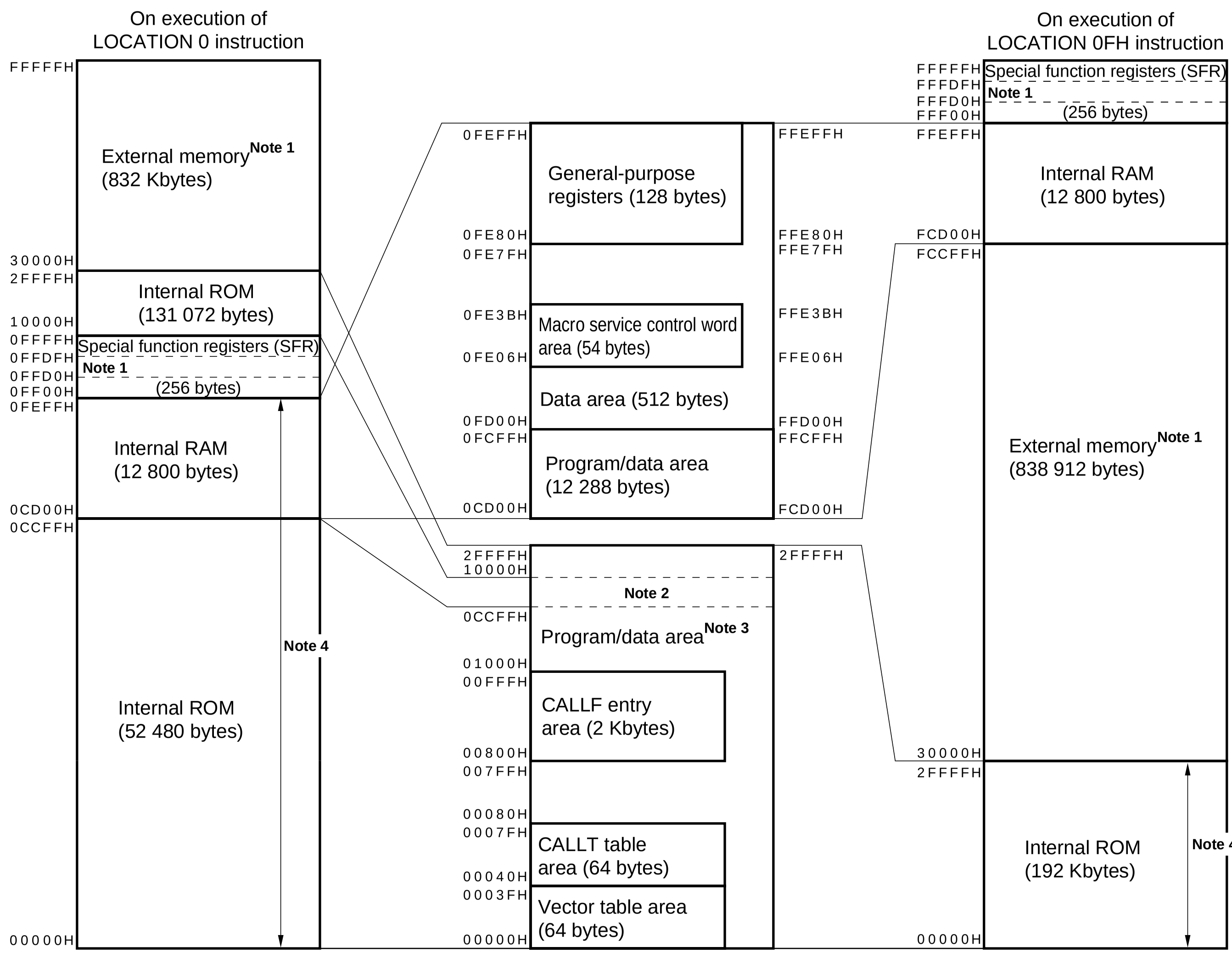
  The internal data area and internal ROM area are mapped as follows:

Part Number	Internal Data Area	Internal ROM Area
μPD784217Y	FCD00H to FFFFFH	00000H to 2FFFFH
μPD784218Y		00000H to 3FFFFH

- **External memory**

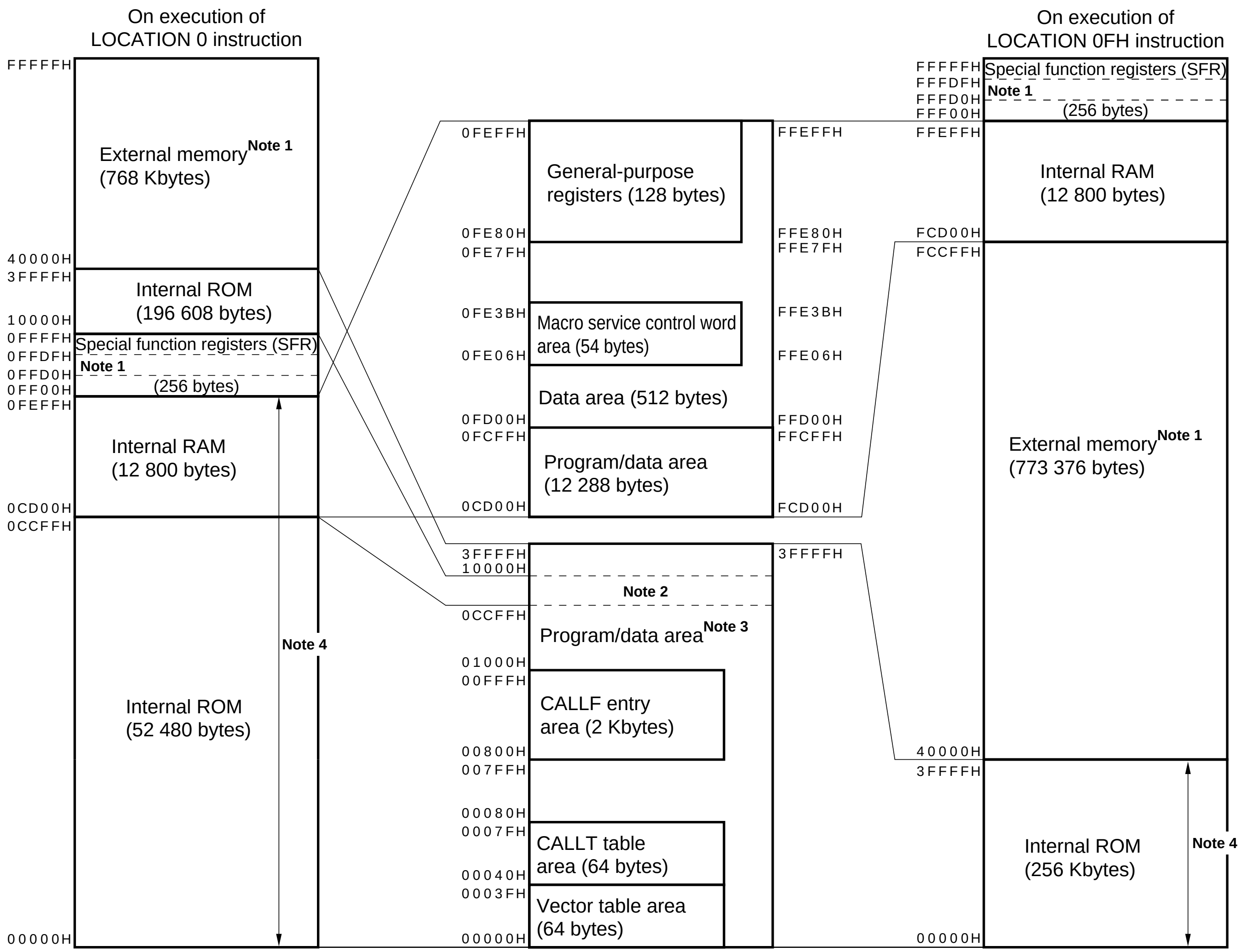
  The external memory is accessed in external memory expansion mode.

Figure 7-1. Memory Map of μPD784217Y



Notes
1. Accessed in external memory expansion mode.
2. This 13 056-byte area can be used as an internal ROM only when the LOCATION 0FH instruction is executed.
3. On execution of LOCATION 0 instruction: 183 552 bytes, on execution of LOCATION 0FH instruction: 196 608 bytes
4. Base area and entry area for reset or interrupt. However, the internal RAM area is not used as a reset entry area.

Figure 7-2. Memory Map of μPD784218Y



Notes **1.** Accessed in external memory expansion mode.

2. This 13 056-byte area can be used as an internal ROM only when the LOCATION 0FH instruction is executed.

3. On execution of LOCATION 0 instruction: 249 088 bytes, on execution of LOCATION 0FH instruction: 262 144 bytes

4. Base area and entry area for reset or interrupt. However, the internal RAM area is not used as a reset entry area.

7.2 CPU Registers

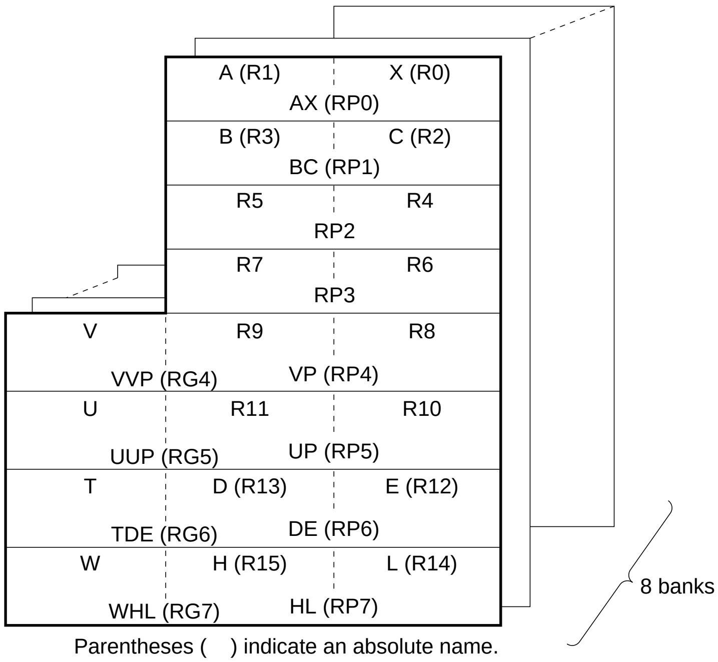
7.2.1 General-purpose registers

Sixteen 8-bit general-purpose registers are available. Two 8-bit registers can be also used in pairs as a 16-bit register. Of the 16-bit registers, four can be used in combination with an 8-bit register for address expansion as 24-bit address specification registers.

Eight banks of these register sets are available which can be selected by using software or the context switching function.

The general-purpose registers except V, U, T, and W registers for address expansion are mapped to the internal RAM.

Figure 7-3. General-Purpose Register Format



Parentheses ( ) indicate an absolute name.

Caution Registers R4, R5, R6, R7, RP2, and RP3 can be used as X, A, C, B, AX, and BC registers, respectively, by setting the RSS bit of the PSW to 1. However, use this function only for recycling the program of the 78K/III Series.

7.2.2 Control registers

(1) Program counter (PC)

The program counter is a 20-bit register whose contents are automatically updated when the program is executed.

Figure 7-4. Program Counter (PC) Format

	19 … 0
PC	

(2) Program status word (PSW)

This register holds the status of the CPU. Its contents are automatically updated when the program is executed.

Figure 7-5. Program Status Word (PSW) Format

PSW		15	14	13	12	11	10	9	8
	PSWH	UF	RBS2	RBS1	RBS0	–	–	–	–

PSW		7	6	5	4	3	2	1	0
	PSWL	S	Z	RSS[Note]	AC	IE	P/V	0	CY

Note This flag is provided to maintain compatibility with the 78K/III Series. Be sure to clear this flag to 0, except when the software for the 78K/III Series is used.

(3) Stack pointer (SP)

This is a 24-bit pointer that holds the first address of the stack. Be sure to write 0 to the higher 4 bits of this pointer.

Figure 7-6. Stack Pointer (SP) Format

	23				20 … 0
SP	0	0	0	0	

8. PERIPHERAL HARDWARE FUNCTIONS

8.1 Ports

The ports shown in Figure 8-1 are provided to make various control operations possible. Table 8-1 shows the function of each port. Ports 0, 2 through 8, 10, 12 can be connected to internal pull-up resistors by software when inputting.

Figure 8-1. Port Configuration

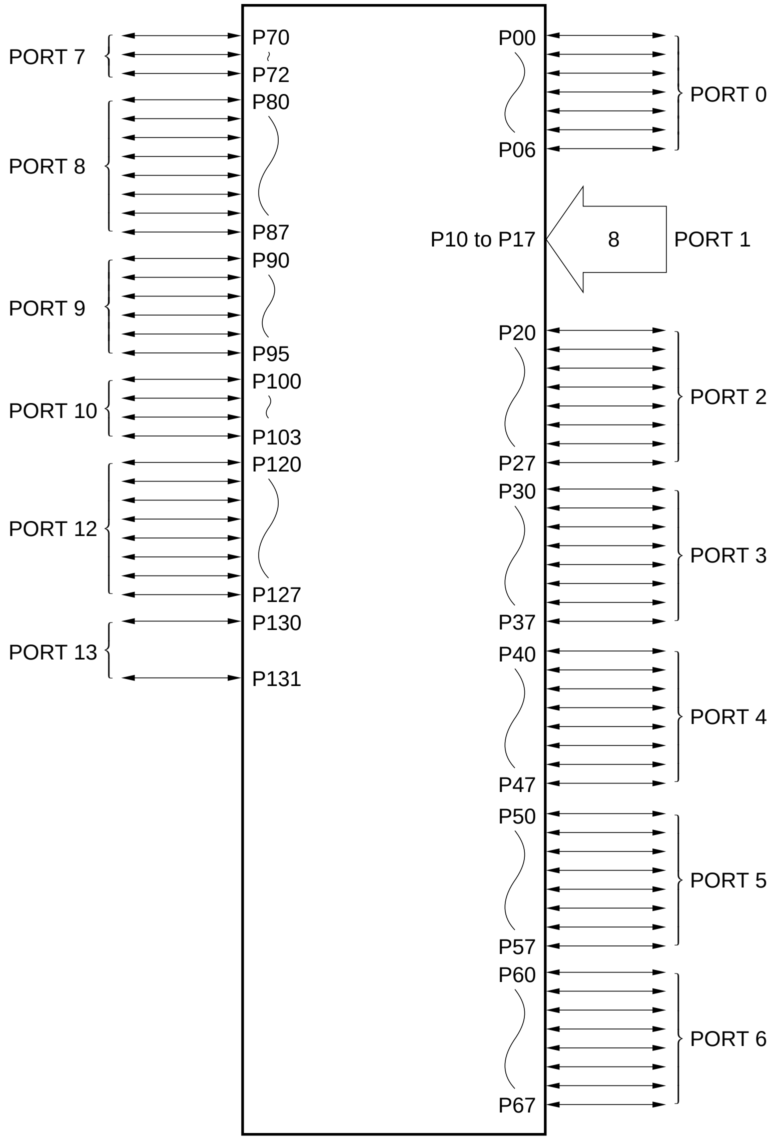


Table 8-1. Port Functions

Port Name	Pin Name	Function	Specification of Pull-up Resistor Connection by Software
Port 0	P00 to P06	• Can be set in input or output mode bit-wise	Can be specified bit-wise
Port 1	P10 to P17	• Input port	—
Port 2	P20 to P27	• Can be set in input or output mode bit-wise	Can be specified bit-wise
Port 3	P30 to P37	• Can be set in input or output mode bit-wise	Can be specified bit-wise
Port 4	P40 to P47	• Can be set in input or output mode bit-wise • Can directly drive LEDs	Can be specified in 1-port units
Port 5	P50 to P57	• Can be set in input or output mode bit-wise • Can directly drive LEDs	Can be specified in 1-port units
Port 6	P60 to P67	• Can be set in input or output mode bit-wise	Can be specified in 1-port units
Port 7	P70 to P72	• Can be set in input or output mode bit-wise	Can be specified bit-wise
Port 8	P80 to P87	• Can be set in input or output mode bit-wise	Can be specified bit-wise
Port 9	P90 to P95	• N-ch open-drain I/O port • Can be set in input or output mode bit-wise • Can directly drive LEDs	—
Port 10	P100 to P103	• Can be set in input or output mode bit-wise	Can be specified bit-wise
Port 12	P120 to P127	• Can be set in input or output mode bit-wise	Can be specified bit-wise
Port 13	P130, P131	• Can be set in input or output mode bit-wise	—

8.2 Clock Generation Circuit

An on-chip clock generation circuit necessary for operation is provided. This clock generation circuit has a divider circuit. If high-speed operation is not necessary, the internal operating frequency can be lowered by the divider circuit to reduce the current consumption.

Figure 8-2. Block Diagram of Clock Generation Circuit

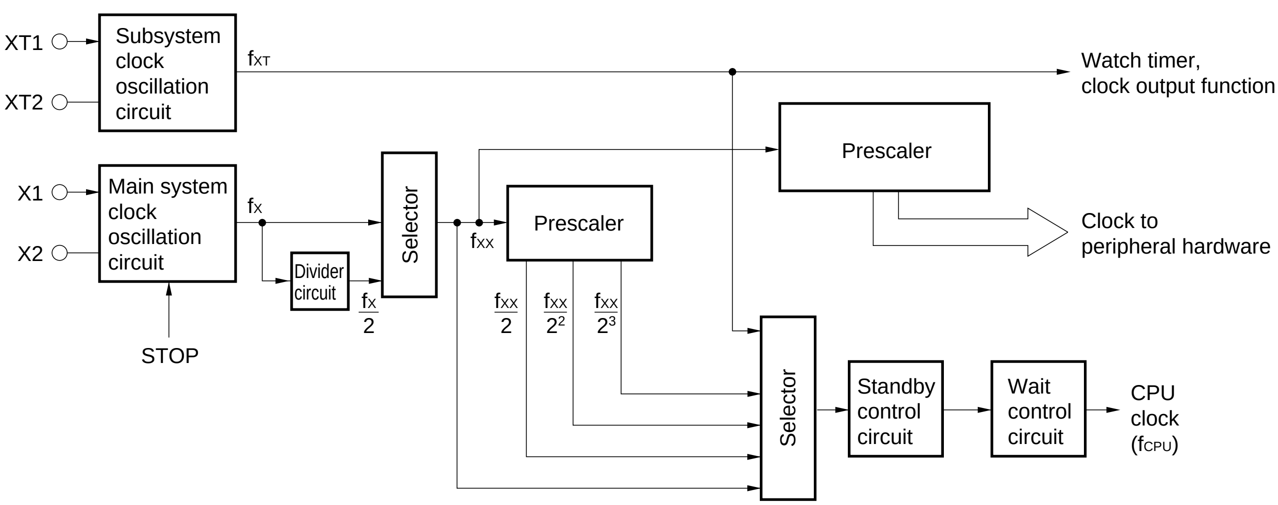
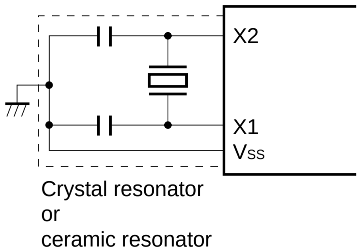


Figure 8-3. Example of Using Main System Clock Oscillation Circuit

(1) Crystal/ceramic oscillation



(2) External clock

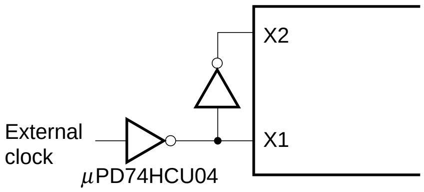
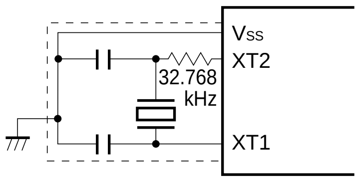
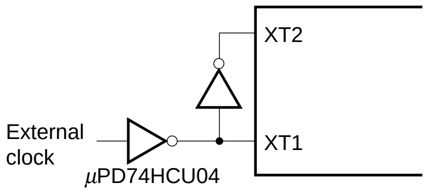


Figure 8-4. Example of Using Subsystem Clock Oscillation Circuit

(1) Crystal oscillation



(2) External clock



Caution When using the main system clock and subsystem clock oscillation circuits, wire the dotted portions in Figures 8-3 and 8-4 as follows to avoid adverse influence from wiring capacitance.

- **Keep the wiring length as short as possible.**
- **Do not cross the wiring with other signal lines.**
- **Do not route the wiring in the vicinity of lines through which a high alternating current flows.**
- **Always keep the potential at the ground point of the capacitor in the oscillation circuit the same as V_{SS}. Do not ground to a ground pattern through which a high current flows.**
- **Do not extract signals from the oscillation circuit.**

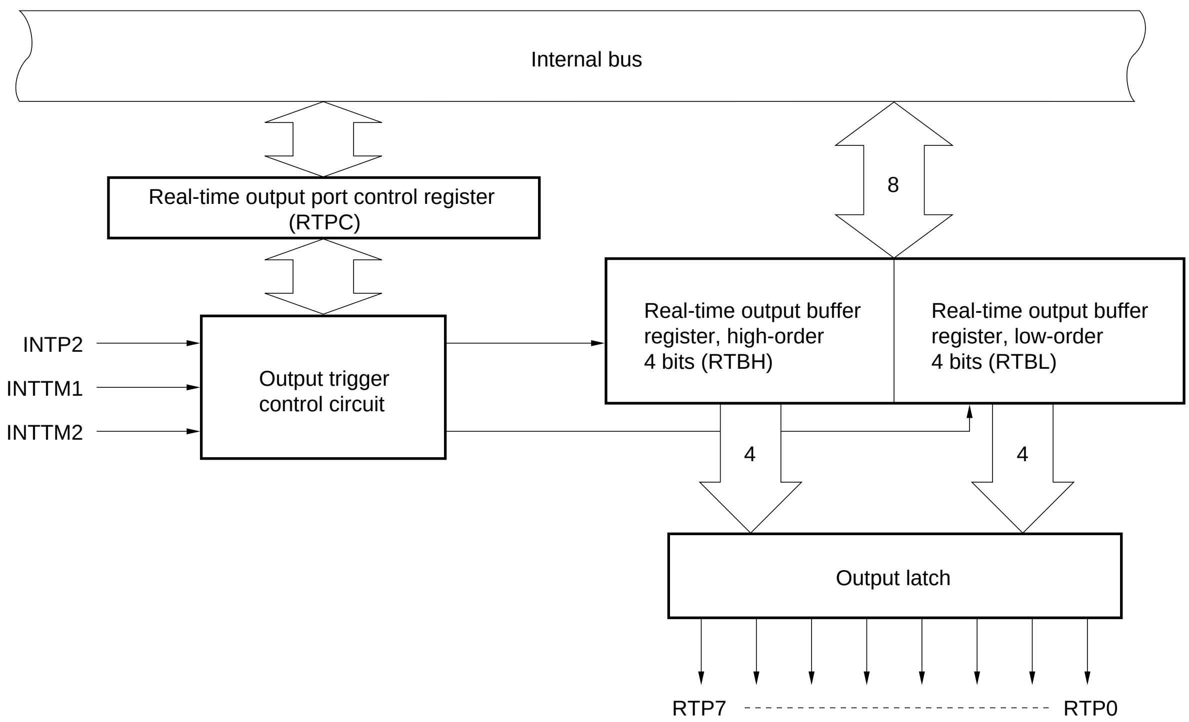
Note that the subsystem clock oscillation circuit has a low amplification factor to reduce the current consumption.

8.3 Real-Time Output Port

The real-time output function is to transfer data set in advance to the real-time output buffer register to the output latch by hardware as soon as the timer interrupt or external interrupt has occurred in order to output the data to an external device. The pins that output the data to the external device constitute a port called a real-time output port.

Because the real-time output port can output signals without jitter, it is ideal for controlling a stepping motor, etc.

Figure 8-5. Block Diagram of Real-Time Output Port



8.4 Timer/Counter

One unit of 16-bit timers/counters and six units of 8-bit timers/counters are provided.

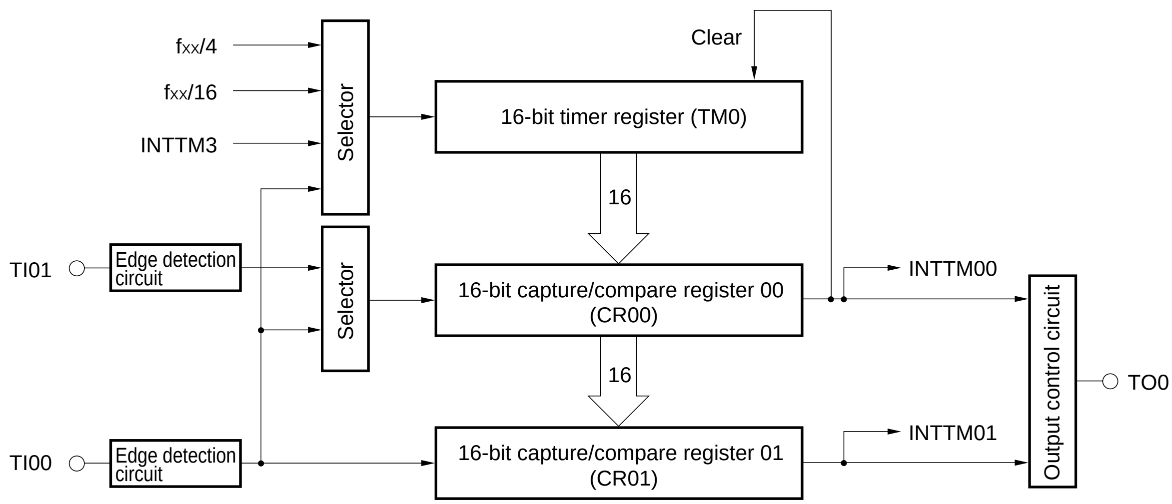
Because a total of eight interrupt requests are supported, these timers/counters can be used as eight units of timers/counters.

Table 8-2. Operations of Timers/Counters

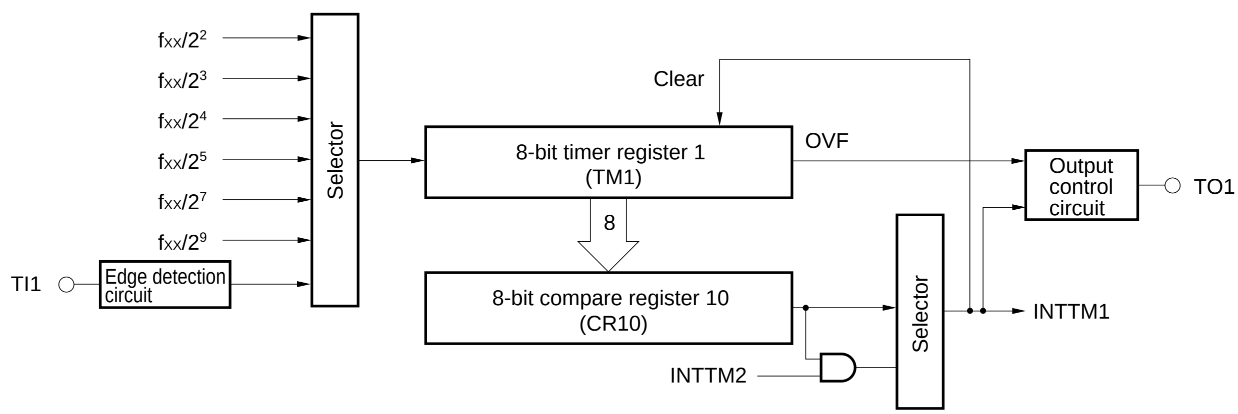
Item	Name	16-Bit Timer/ Counter	8-Bit Timer/ Counter 1	8-Bit Timer/ Counter 2	8-Bit Timer/ Counter 5	8-Bit Timer/ Counter 6	8-Bit Timer/ Counter 7	8-Bit Timer/ Counter 8
Count width	8 bits	—	○	○	○	○	○	○
	16 bits	○	○		○		○	
Operation mode	Interval timer	1ch	1ch	1ch	1ch	1ch	1ch	1ch
	External event counter	○	○	○	○	○	○	○
Function	Timer output	1ch	1ch	1ch	1ch	1ch	1ch	1ch
	PPG output	○	—	—	—	—	—	—
	PWM output	○	○	○	○	○	○	○
	Square wave output	○	○	○	○	○	○	○
	One-shot pulse output	○	—	—	—	—	—	—
	Pulse width measurement	2 inputs	—	—	—	—	—	—
	Number of interrupt requests	2	1	1	1	1	1	1

Figure 8-6. Block Diagram of Timers/Counters (1/2)

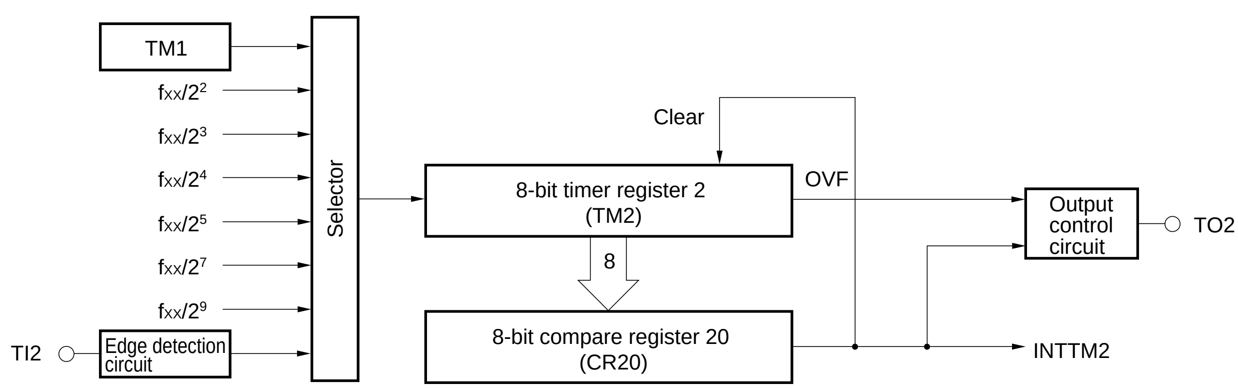
16-bit timer/counter



8-bit timer/counter 1



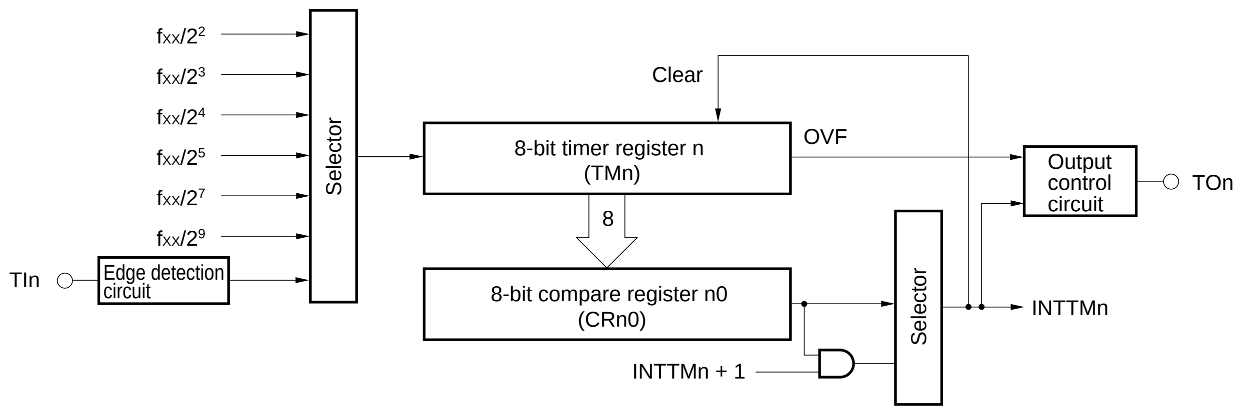
8-bit timer/counter 2



Remark OVF: overflow flag

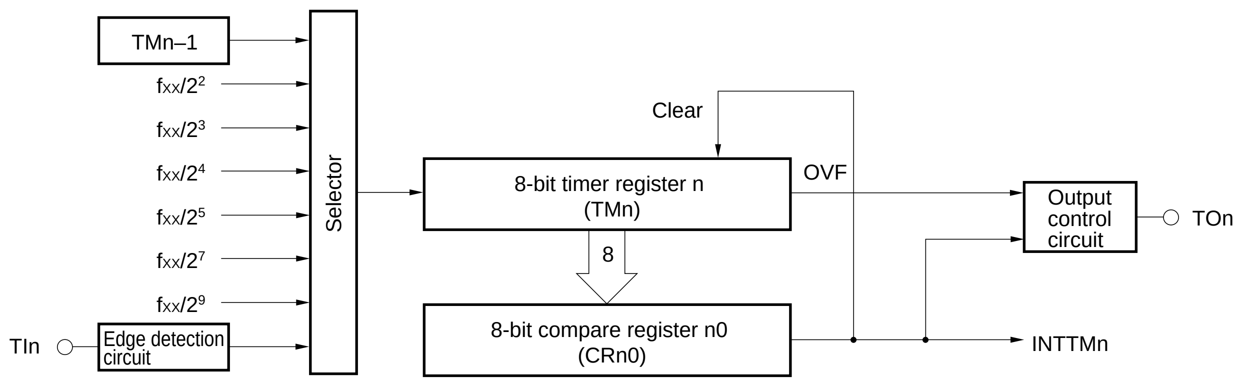
Figure 8-6. Block Diagram of Timers/Counters (2/2)

8-bit timer/counter 5, 7



Remark n = 5, 7

8-bit timer/counter 6, 8



Remark n = 6, 8

8.5 A/D Converter

An A/D converter converts an analog input variable into a digital signal. This microcontroller is provided with an A/D converter with a resolution of 8 bits and 8 channels (ANI0 through ANI7).

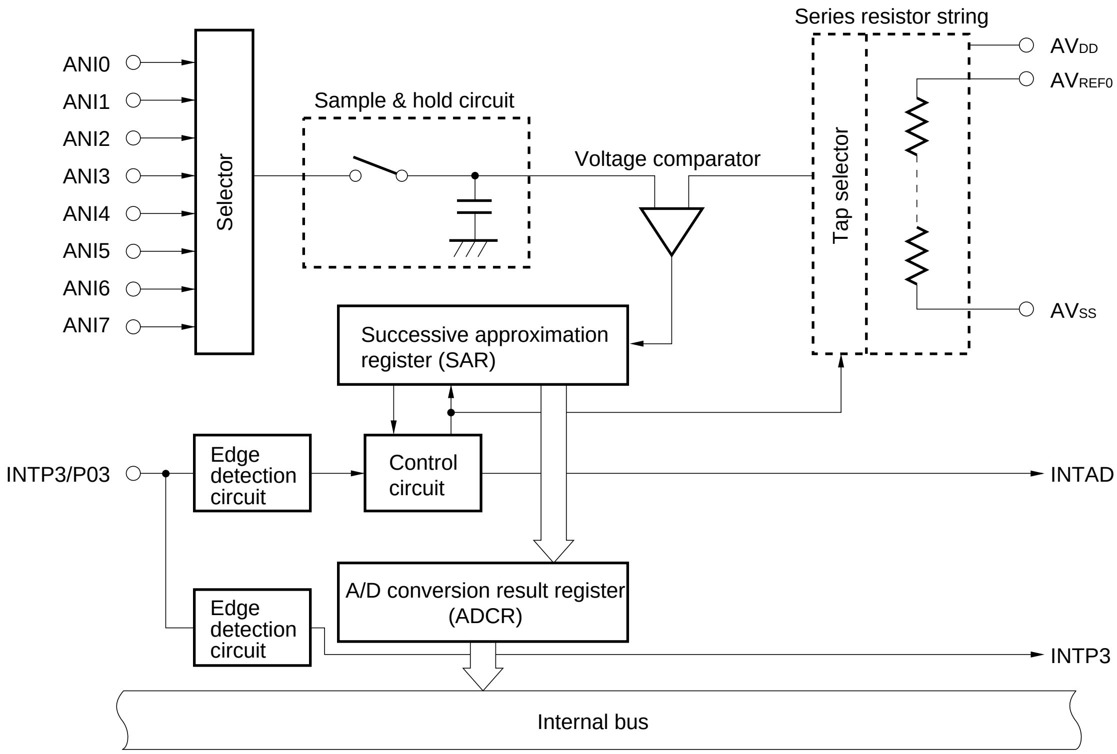
This A/D converter is of successive approximation type and the result of conversion is stored to an 8-bit A/D conversion result register (ADCR).

The A/D converter can be started in the following two ways:

- Hardware start
  Conversion is started by trigger input (P03).
- Software start
  Conversion is started by setting the A/D converter mode register.

One analog input channel is selected from ANI0 through ANI7 for A/D conversion. When A/D conversion is started by means of hardware start, conversion is stopped after it has been completed. When conversion is started by means of software start, A/D conversion is repeatedly executed, and each time conversion has been completed, an interrupt request (INTAD) is generated.

Figure 8-7. Block Diagram of A/D Converter



8.6 D/A Converter

A D/A converter converts an input digital signal into an analog voltage. This microcontroller is provided with a voltage output type D/A converter with a resolution of 8 bits and two channels.

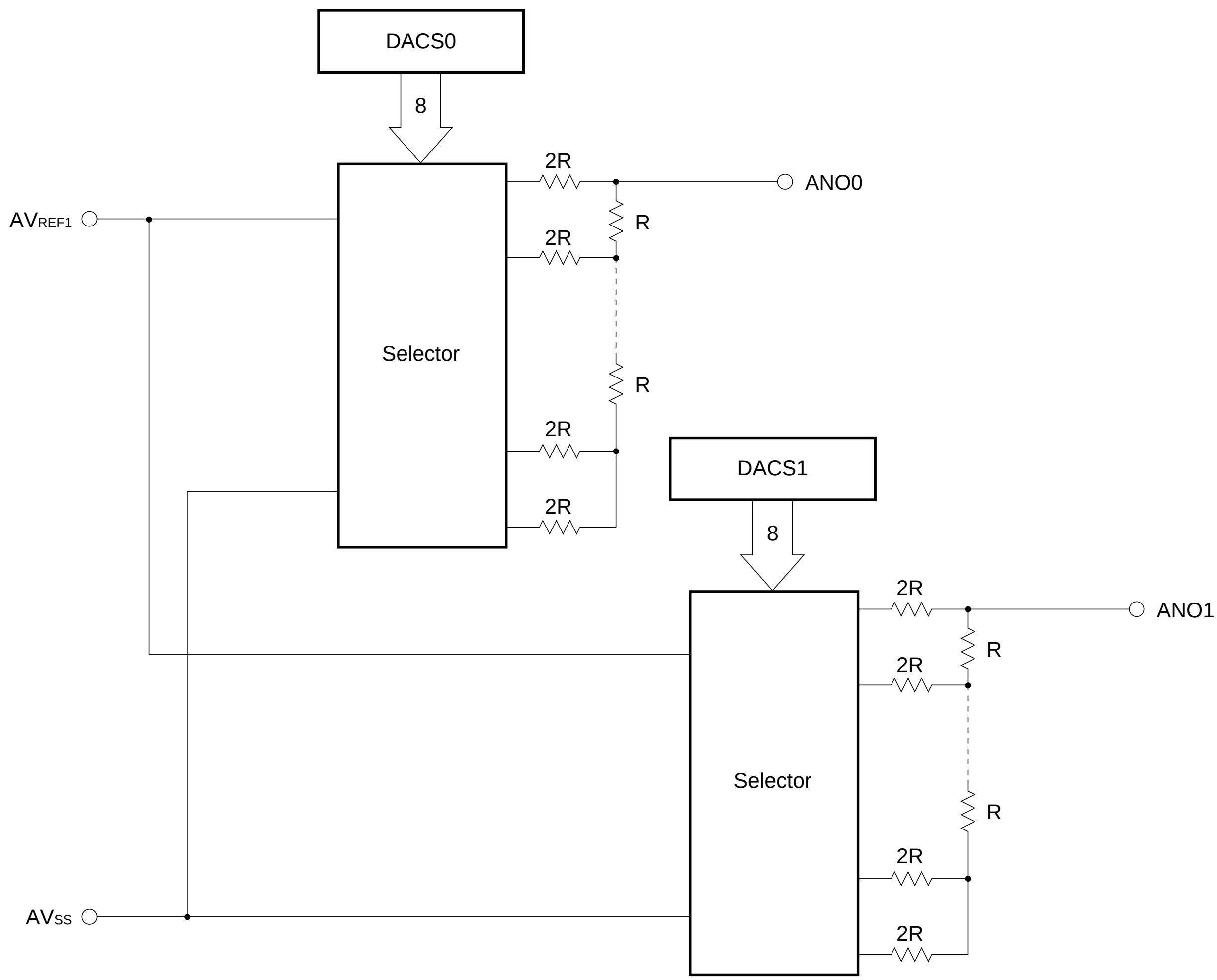
The conversion method is of R-2R resistor ladder type.

D/A conversion is started by setting DACE0 of the D/A converter mode register 0 (DAM0) and DACE1 of the D/A converter mode register 1 (DAM1).

The D/A converter operates in the following two modes:

- Normal mode
  The converter outputs an analog voltage immediately after it has completed D/A conversion.
- Real-time output mode
  The converter outputs an analog voltage in synchronization with an output trigger after it has completed D/A conversion.

Figure 8-8. Block Diagram of D/A Converter



8.7 Serial Interface

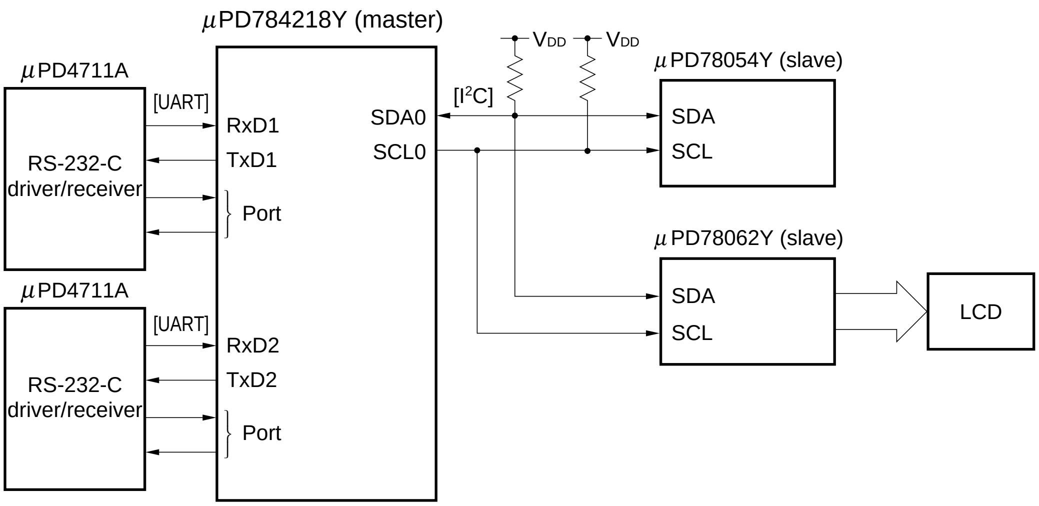
Three independent serial interface channels are provided.

- Asynchronous serial interface (UART)/3-wire serial I/O (IOE) × 2
- Clocked serial interface (CSI) × 1
  - 3-wire serial I/O (IOE)
  - I^2C bus interface (I^2C)

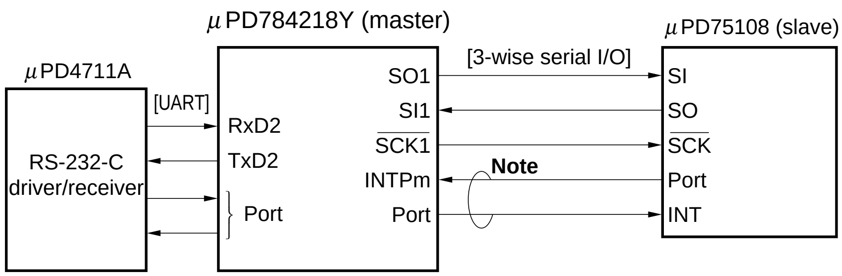
Therefore, communication with an external system and local communication within the system can be simultaneously executed (refer to **Figure 8-9**).

Figure 8-9. Example of Serial Interface

(a) UART + I^2C



(b) UART + 3-wire serial I/O



Note Handshake line

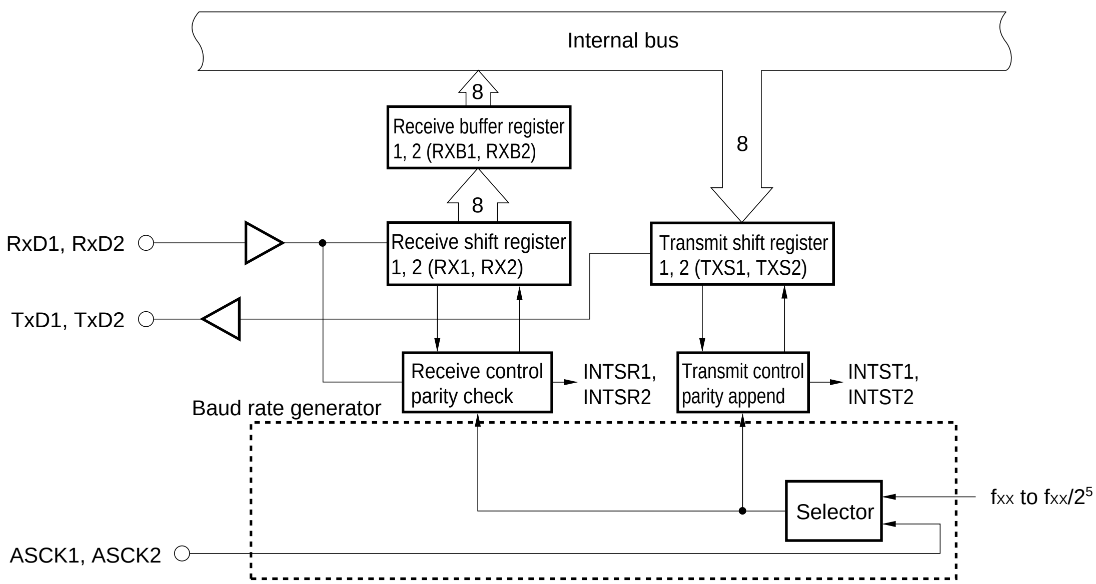
8.7.1 Asynchronous serial interface/3-wire serial I/O (UART/IOE)

Two channels of serial interfaces that can select an asynchronous serial interface mode and 3-wire serial I/O mode are provided.

(1) Asynchronous serial interface mode

In this mode, data of 1 byte following the start bit is transmitted or received.
Because an on-chip baud rate generator is provided, a wide range of baud rates can be set.
Moreover, the clock input to the ASCK pin can be divided to define a baud rate.
When the baud rate generator is used, a baud rate conforming to the MIDI standard (31.25 kbps) can be also obtained.

Figure 8-10. Block Diagram in Asynchronous Serial Interface Mode

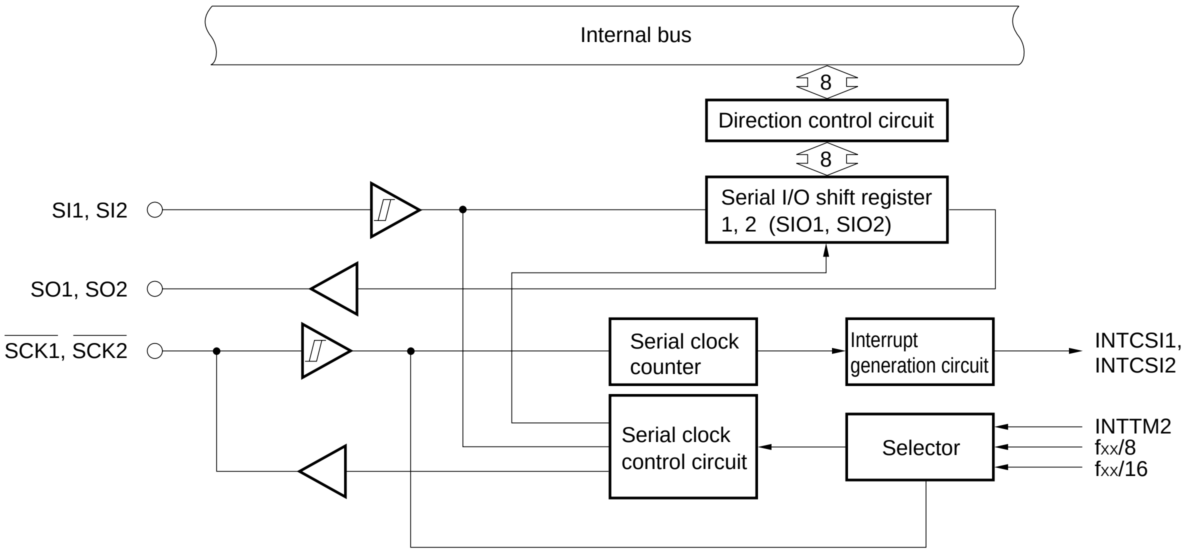


(2) 3-wire serial I/O mode

In this mode, the master device starts transfer by making the serial clock active and communicates 1-byte data in synchronization with this clock.

This mode is used to communicate with a device having the conventional clocked serial interface. Basically, communication is established by using three lines: serial clocks ($\overline{SCK1}$ and $\overline{SCK2}$), serial data inputs (SI1 and SI2), and serial data outputs (SO1 and SO2). To connect two or more devices, a handshake line is necessary.

Figure 8-11. Block Diagram in 3-wire Serial I/O Mode



8.7.2 Clocked serial interface (CSI)

In this mode, the master device starts transfer by making the serial clock active and communicates 1-byte data in synchronization with this clock.

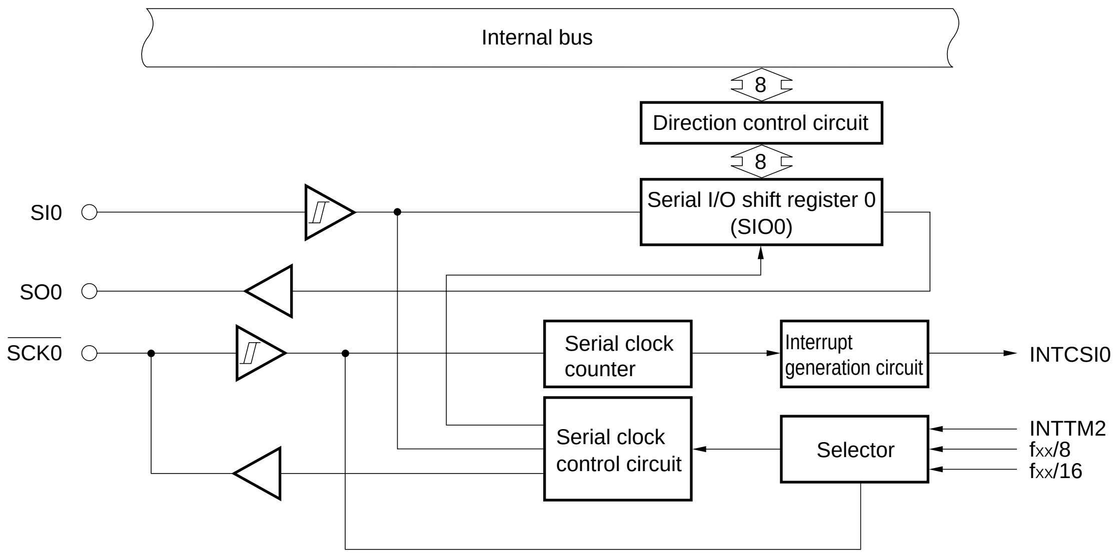
(1) 3-wire serial I/O mode

This mode is to communicate with devices having the conventional clocked serial interface.

Basically, communication is established in this mode with three lines: one serial clock ($\overline{SCK0}$) and two serial data (SI0 and SO0) lines.

Generally, a handshake line is necessary to check the reception status.

Figure 8-12. Block Diagram in 3-wire Serial I/O Mode



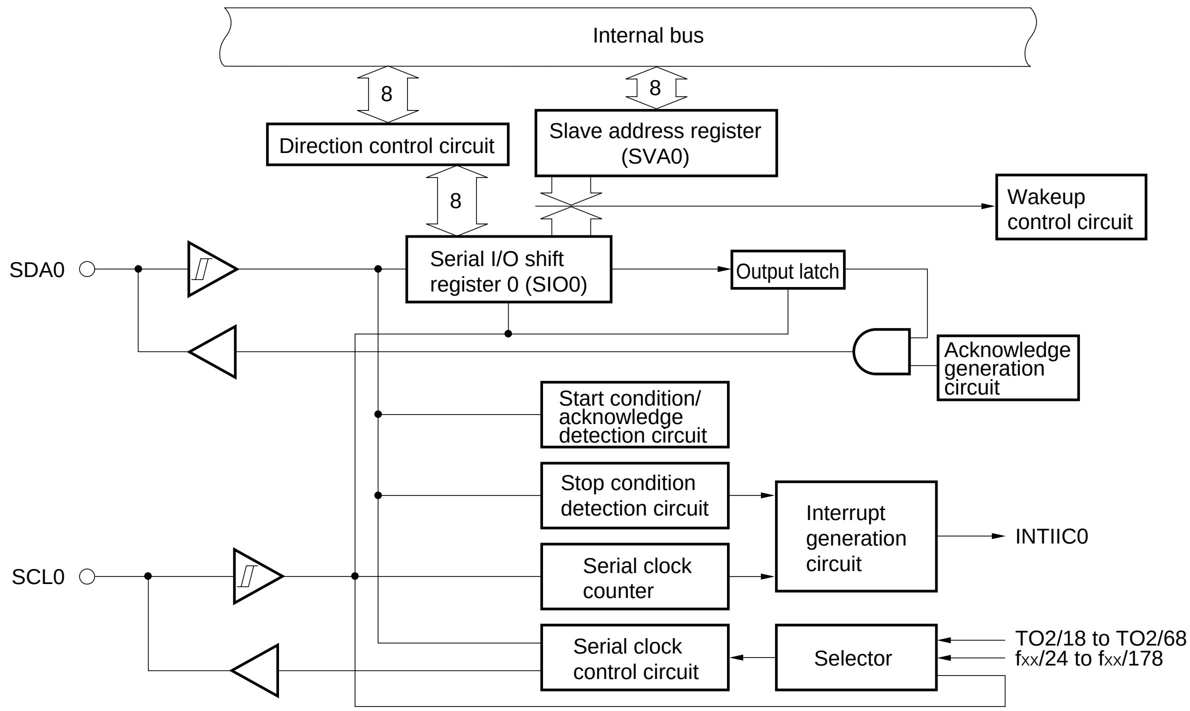
(2) I²C (Inter IC) bus mode (Multi-master supporting)

This mode is to communicate with devices conforming to the I²C bus format.

This mode is to transfer 8-bit data with two or more devices by using two lines: serial clock (SCL0) and serial data bus (SDA0).

During transfer, a “start condition”, “data”, and “stop condition” can be output onto the serial data bus. During reception, these data can be automatically detected by hardware.

Figure 8-13. Block Diagram in I²C Bus Mode

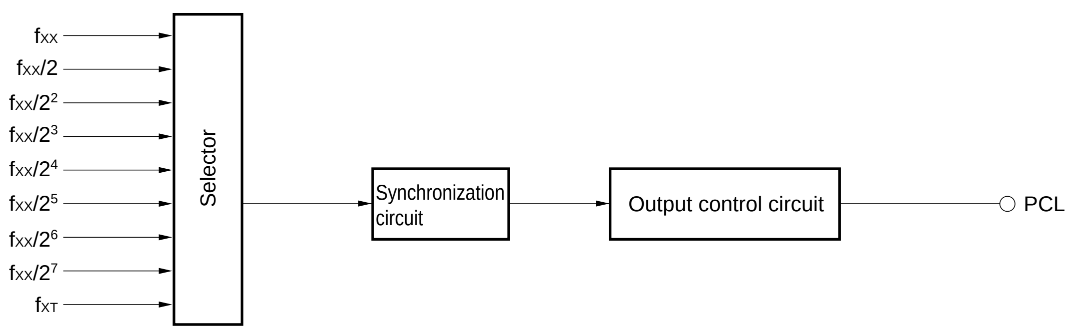


8.8 Clock Output Function

Clocks of the following frequencies can be output as clock output.

- 97.7 kHz/195 kHz/391 kHz/781 kHz/1.56 MHz/3.13 MHz/6.25 MHz/12.5 MHz (main system clock: 12.5 MHz)
- 32.768 kHz (subsystem clock: 32.768 kHz)

Figure 8-14. Block Diagram of Clock Output Function

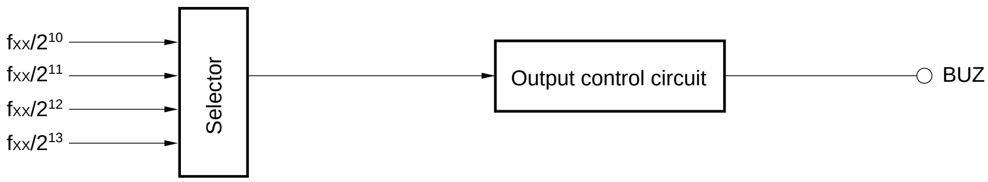


8.9 Buzzer Output Function

Clocks of the following frequencies can be output as buzzer output.

• 1.5 kHz/3.1 kHz/6.1 kHz/12.2 kHz (main system clock: 12.5 MHz)

Figure 8-15. Block Diagram of Buzzer Output Function



8.10 Edge Detection Function

The interrupt input pins (INTP0, INTP1, NMI/INTP2, INTP3 through INTP6) are used not only to input interrupt requests but also to input trigger signals to the internal hardware units. Because these pins operate at an edge of the input signal, they have a function to detect an edge. Moreover, a noise reduction circuit is also provided to prevent erroneous detection due to noise.

Pin Name	Detectable Edge	Noise Reduction
NMI	Either or both of rising and falling edges	By analog delay
INTP0 through INTP6		

8.11 Watch Timer

The watch timer has the following functions:

• Watch timer
• Interval timer

The watch timer and interval timer functions can be used at the same time.

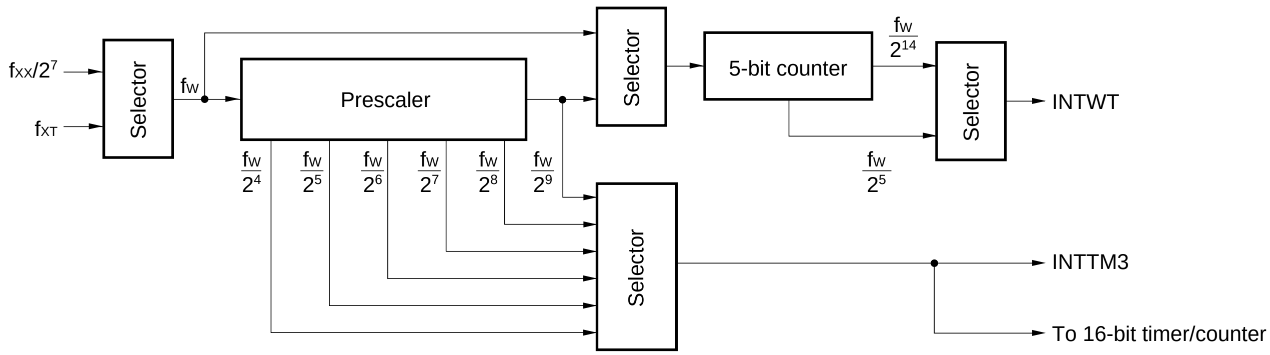
(1) Watch timer

The watch timer sets the WTIF flag of the interrupt control register (WTIC) at time intervals of 0.5 seconds by using the 32.768-kHz subsystem clock.

(2) Interval timer

The interval timer generates an interrupt request (INTTM3) at predetermined time intervals.

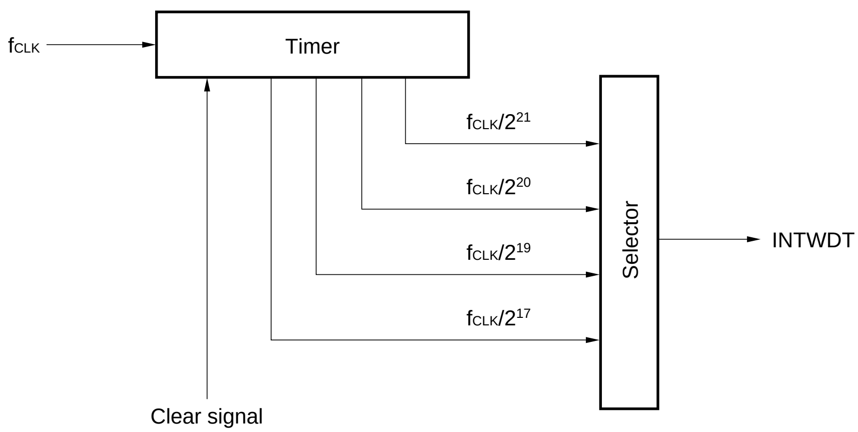
Figure 8-16. Block Diagram of Watch Timer



8.12 Watchdog Timer

A watchdog timer is provided to detect a hang up of the CPU. This watchdog timer generates a non-maskable or maskable interrupt unless it is cleared by software within a specified interval time. Once enabled to operate, the watchdog timer cannot be stopped by software. Whether the interrupt by the watchdog timer or the interrupt input from the NMI pin takes precedence can be specified.

Figure 8-17. Block Diagram of Watchdog Timer



Remark f_{CLK}: Internal system clock (f_{XX} to $f_{XX}/8$)

9. INTERRUPT FUNCTION

As the servicing in response to an interrupt request, the three types shown in Table 9-1 can be selected by program.

Table 9-1. Servicing of Interrupt Request

Servicing Mode	Entity of Servicing	Servicing	Contents of PC and PSW
Vectored interrupt	Software	Branches and executes servicing routine (servicing is arbitrary)	Saves to and restores from stack
Context switching		Automatically switches register bank, branches and executes servicing routine (servicing is arbitrary)	Saves to or restores from fixed area in register bank
Macro service	Firmware	Executes data transfer between memory and I/O (servicing is fixed)	Retained

9.1 Interrupt Sources

Table 9-2 shows the interrupt sources available. As shown, interrupts are generated by 29 types of sources, execution of the BRK instruction, BRKCS instruction, or an operand error.

The priority of interrupt servicing can be set to four levels, so that nesting can be controlled during interrupt servicing and that which of the two or more interrupts that simultaneously occur should be serviced first. When the macro service function is used, however, nesting always proceeds.

The default priority is the priority (fixed) of the service that is performed if two or more interrupt requests, having the same priority, simultaneously generate (refer to **Table 9-2**).

Table 9-2. Interrupt Sources

Type	Default Priority	Source		Internal/ External	Macro Service
		Name	Trigger		
Software	—	BRK instruction	Instruction execution	—	—
		BRKCS instruction	Instruction execution		
		Operand error	If result of exclusive OR between operands byte and $\overline{\text{byte}}$ is not FFH when MOV STBC, #byte instruction, MOV WDM, #byte instruction, or LOCATION instruction is executed		
Non-maskable	—	NMI	Pin input edge detection	External	—
		INTWDT	Overflow of watchdog timer	Internal	
Maskable	0 (highest)	INTWDTM	Overflow of watchdog timer	Internal	○
	1	INTP0	Pin input edge detection	External	
	2	INTP1			
	3	INTP2			
	4	INTP3			
	5	INTP4			
	6	INTP5			
	7	INTP6			
	8	INTIIC0	End of I^2C bus transfer by CSI0	Internal	
		INTCSI0	End of 3-wire transfer by CSI0		
	9	INTSER1	Occurrence of UART reception error in ASI1		
	10	INTSR1	End of UART reception by ASI1		
		INTCSI1	End of 3-wire transfer by CSI1		
	11	INTST1	End of UART transmission by ASI1		
	12	INTSER2	Occurrence of UART reception error in ASI2		
	13	INTSR2	End of UART reception by ASI2		
		INTCSI2	End of 3-wire transfer by CSI2		
	14	INTST2	End of UART transmission by ASI2		
	15	INTTM3	Reference time interval signal from watch timer		
	16	INTTM00	Signal indicating coincidence between 16-bit timer register and capture/compare register (CR00)		
	17	INTTM01	Signal indicating coincidence between 16-bit timer register and capture/compare register (CR01)		
	18	INTTM1	Occurrence of coincidence signal of 8-bit timer/counter 1		
	19	INTTM2	Occurrence of coincidence signal of 8-bit timer/counter 2		
	20	INTAD	End of conversion by A/D converter		
	21	INTTM5	Occurrence of coincidence signal of 8-bit timer/counter 5		
	22	INTTM6	Occurrence of coincidence signal of 8-bit timer/counter 6		
	23	INTTM7	Occurrence of coincidence signal of 8-bit timer/counter 7		
	24	INTTM8	Occurrence of coincidence signal of 8-bit timer/counter 8		
	25	INTWT	Overflow of watch timer		
	26 (lowest)	INTKR	Detection of falling edge of port 8	External	

Remark ASI : Asynchronous Serial Interface
CSI : Clocked Serial Interface

9.2 Vectored Interrupt

Execution branches to a servicing routine by using the memory contents of a vector table address corresponding to the interrupt source as the address of the branch destination.

So that the CPU performs interrupt servicing, the following operations are performed:

- On branching: Saves the status of the CPU (contents of PC and PSW) to stack
- On returning : Restores the status of the CPU (contents of PC and PSW) from stack

To return to the main routine from an interrupt service routine, the RETI instruction is used.

The branch destination address is in a range of 0 to FFFFH.

Table 9-3. Vector Table Address

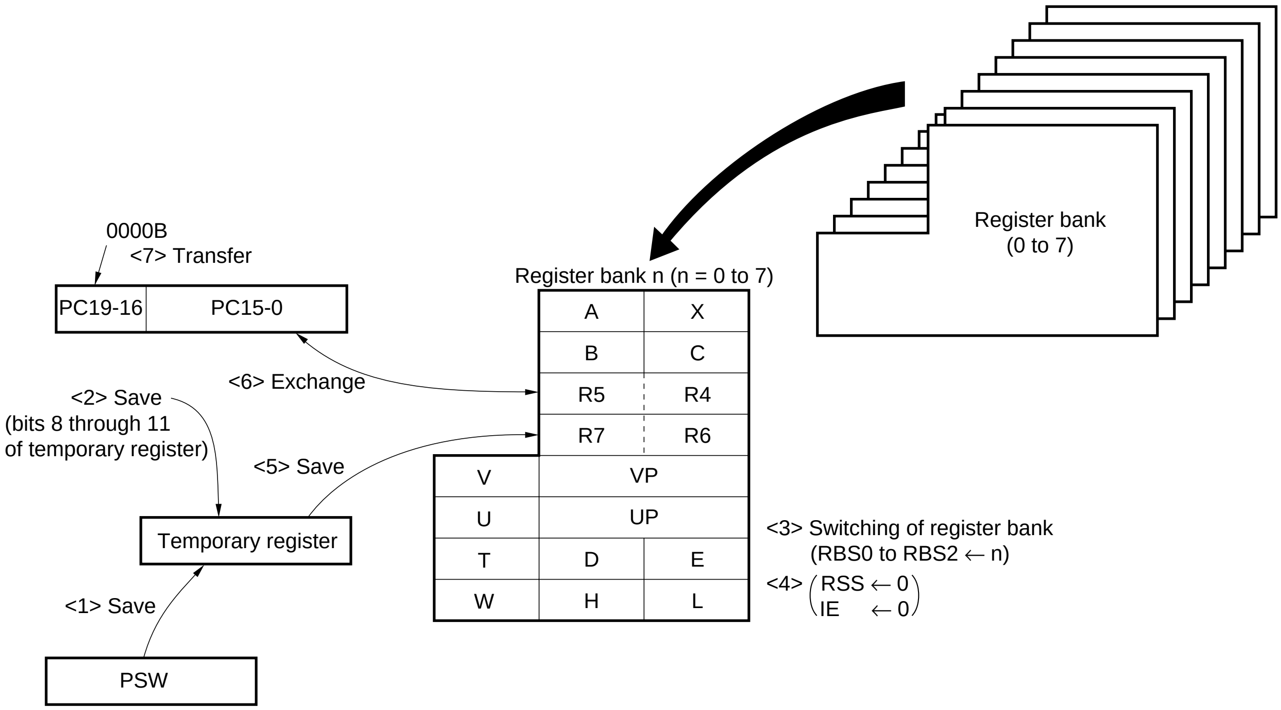
Interrupt Source	Vector Table Address	Interrupt Source	Vector Table Address
BRK instruction	003EH	INTST1	001CH
Operand error	003CH	INTSER2	001EH
NMI	0002H	INSR2	0020H
INTWDT (non-maskable)	0004H	INTCSI2	
INTWDTM (maskable)	0006H	INTST2	0022H
INTP0	0008H	INTTM3	0024H
INTP1	000AH	INTTM00	0026H
INTP2	000CH	INTTM01	0028H
INTP3	000EH	INTTM1	002AH
INTP4	0010H	INTTM2	002CH
INTP5	0012H	INTAD	002EH
INTP6	0014H	INTTM5	0030H
INTIIC0	0016H	INTTM6	0032H
INTCSI0		INTTM7	0034H
INTSER1	0018H	INTTM8	0036H
INTSR1	001AH	INTWT	0038H
INTCSI1		INTKR	003AH

9.3 Context Switching

When an interrupt request is generated or when the BRKCS instruction is executed, a predetermined register bank is selected by hardware. Context switching is a function that branches execution to a vector address stored in advance in the register bank, and to stack the current contents of the program counter (PC) and program status word (PSW) to the register bank.

The branch destination address is in a range of 0 to FFFFH.

Figure 9-1. Context Switching Operation When Interrupt Request Is Generated

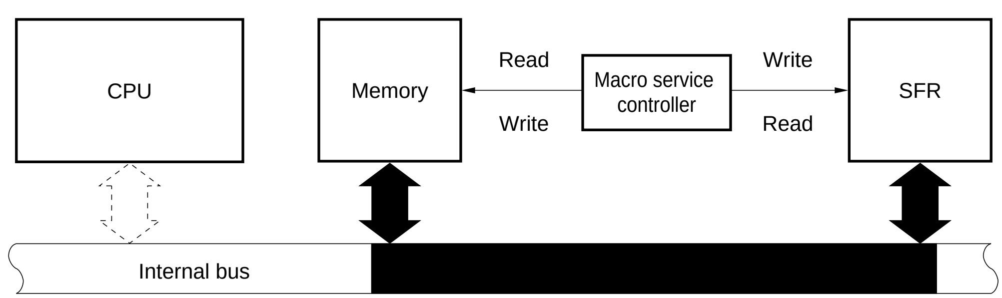


9.4 Macro Service

This function is to transfer data between memory and a special function register (SFR) without intervention by the CPU. A macro service controller accesses the memory and SFR in the same transfer cycle and directly transfers data without loading it.

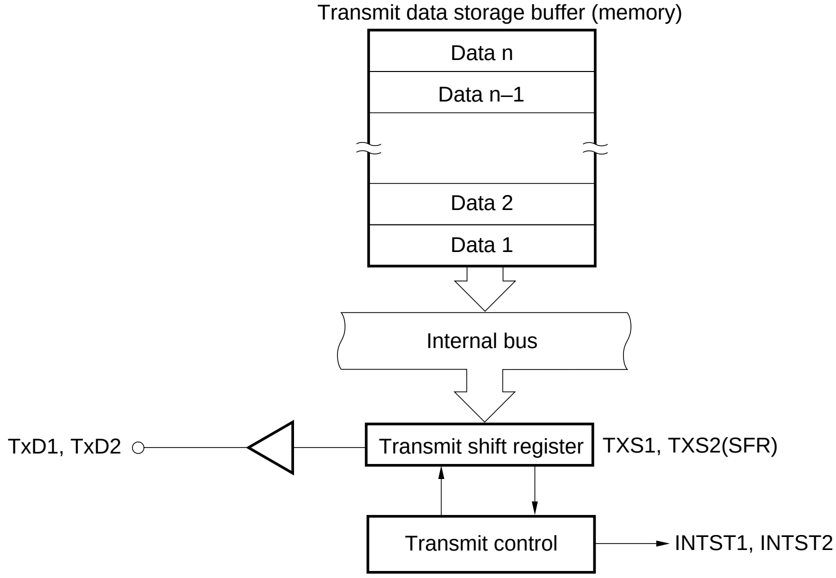
Because this function does not save or restore the status of the CPU, or load data, data can be transferred at high speeds.

Figure 9-2. Macro Service



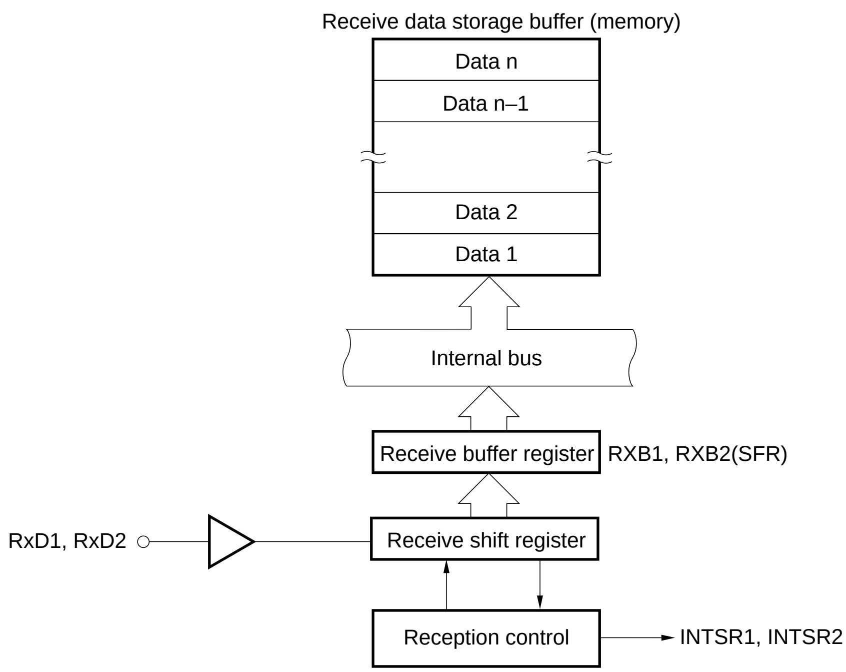
9.5 Application Example of Macro Service

(1) Transmission of serial interface



Each time macro service requests INTST1 and INTST2 are generated, the next transmit data is transferred from memory to TXS1 and TXS2. When data n (last byte) has been transferred to TXS1 and TXS2 (when the transmit data storage buffer has become empty), vectored interrupt requests INTST1 and INTST2 are generated.

(2) Reception of serial interface



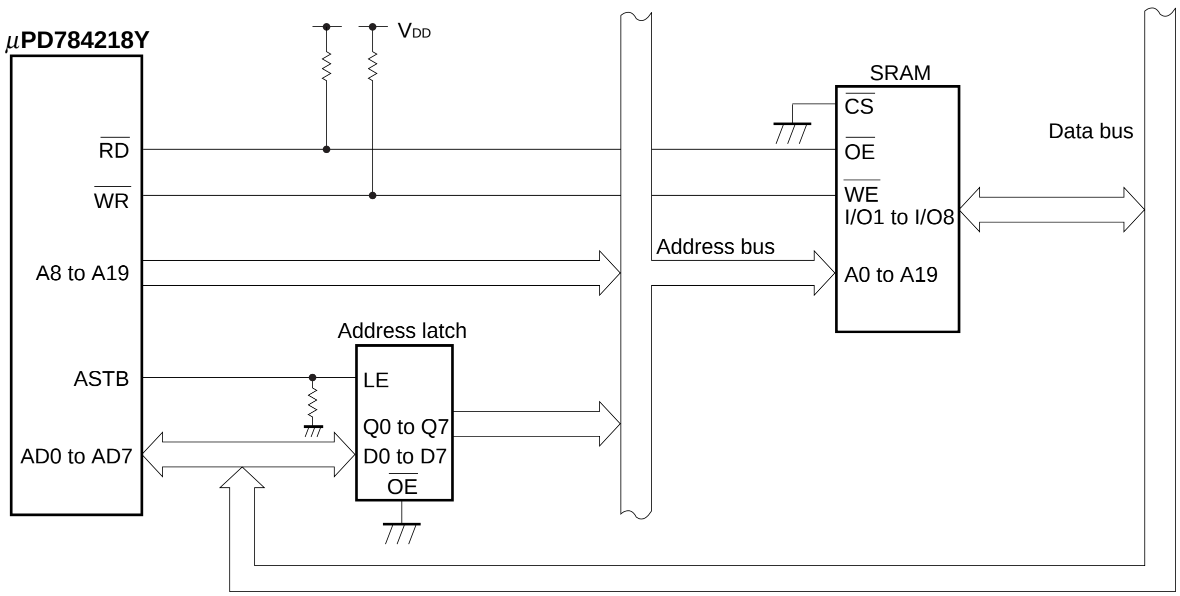
Each time macro service requests INTSR1 and INTSR2 are generated, the receive data is transferred from RXB1 and RXB2 to memory. When data n (last byte) has been transferred to memory (when the receive data storage buffer has become full), vectored interrupt requests INTSR1 and INTSR2 are generated.

10. LOCAL BUS INTERFACE

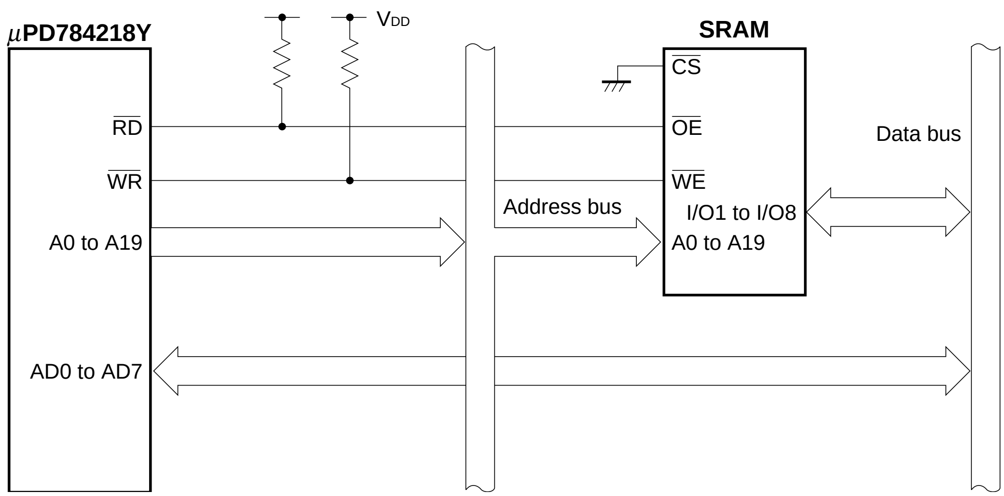
The local bus interface can connect an external memory or I/O (memory mapped I/O) and support a memory space of 1 Mbyte (refer to **Figure 10-1**).

Figure 10-1. Example of Local Bus Interface

(1) Multiplexed bus mode



(2) Separate bus mode



10.1 Memory Expansion

External program memory and data memory can be connected in two stages: 256 Kbytes and 1 Mbyte.

To connect the external memory, ports 4 through 6 and port 8 are used.

The external memory can be connected in the following two modes:

- Multiplexed bus mode: The external memory is connected by using a time-division address/data bus. The number of ports used when the external memory is connected can be reduced in this mode.
- Separate bus mode : The external memory is connected by using an address bus and data bus independent of each other. Because an external latch circuit is not necessary, this mode is useful for reducing the number of components and mounting area on the printed wiring board.

10.2 Programmable Wait

Wait state(s) can be inserted to the memory space (00000H through FFFFFH) while the $\overline{\text{RD}}$ and $\overline{\text{WR}}$ signals are active.

In addition, there is an address wait function that extends the active period of the ASTB signal to gain the address decode time.

10.3 External Access Status Function

The P37/EXA pin outputs an active-low external access status signal. This signal informs the other devices connected with the external bus of the external access status, disables data output to the external bus by the other devices, and enables reception.

The external access status signal is output while the external memory is accessed.

11. STANDBY FUNCTION

This function is to reduce the power dissipation of the chip, and can be used in the following modes:

- HALT mode : Stops supply of the operating clock to the CPU. This mode is used in combination with the normal operation mode for intermittent operation to reduce the average power dissipation.
- IDLE mode : Stops the entire system with the oscillation circuit continuing operation. The power dissipation in this mode is close to that in the STOP mode. However, the time required to restore the normal program operation from this mode is almost the same as that from the HALT mode.
- STOP mode : Stops the main system clock and thereby to stop all the internal operations of the chip. Consequently, the power dissipation is minimized with only leakage current flowing.
- Power-saving mode : The main system clock is stopped with the subsystem clock used as the system clock. The CPU can operate on the subsystem clock to reduce the current consumption.
- Power-saving HALT mode : This is a standby function in the power-saving mode and stops the operation clock of the CPU, to reduce the power dissipation of the entire system.
- Power-saving IDLE mode : This is a standby function in the power-saving mode and stops the entire system except the oscillation circuit, to reduce the power dissipation of the entire system.

These modes are programmable.

In addition, the macro service can be started in the HALT mode or power-saving HALT mode. The HALT mode is restored again after execution of the macro service processing.

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