

## TOSHIBA MOS DIGITAL INTEGRATED CIRCUIT SILICON GATE CMOS

## 524,288-WORD BY 16-BIT/1,048,576-WORD BY 8-BIT FULL CMOS STATIC RAM

**DESCRIPTION**

The TC55W800FT is a 8,388,608-bit static random access memory (SRAM) organized as 524,288 words by 16 bits/1,048,576 words by 8 bits. Fabricated using Toshiba's CMOS Silicon gate process technology, this device operates from a single 2.3 to 3.3 V power supply. Advanced circuit technology provides both high speed and low power at an operating current of 3 mA/MHz and a minimum cycle time of 55 ns. It is automatically placed in low-power mode at 0.5  $\mu$ A standby current (at  $V_{DD} = 3$  V,  $T_a = 25^\circ\text{C}$ , maximum) when chip enable ( $\overline{\text{CE1}}$ ) is asserted high or ( $\overline{\text{CE2}}$ ) is asserted low. There are three control inputs.  $\overline{\text{CE1}}$  and  $\overline{\text{CE2}}$  are used to select the device and for data retention control, and output enable ( $\overline{\text{OE}}$ ) provides fast memory access. Data byte control pin ( $\overline{\text{LB}}$ ,  $\overline{\text{UB}}$ ) provides lower and upper byte access. This device is well suited to various microprocessor system applications where high speed, low power and battery backup are required. And, with a guaranteed operating extreme temperature range of  $-40^\circ$  to  $85^\circ\text{C}$ , the TC55W800FT can be used in environments exhibiting extreme temperature conditions. The TC55W800FT is available in a plastic 48-pin thin-small-outline package (TSOP).

**FEATURES**

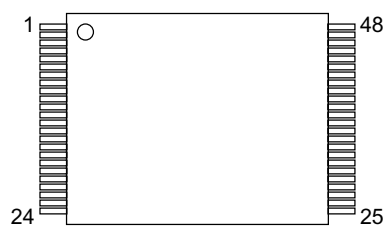
- Low-power dissipation  
Operating: 9.9 mW/MHz (typical)
- Single power supply voltage of 2.3 to 3.3 V
- Power down features using  $\overline{\text{CE1}}$  and  $\overline{\text{CE2}}$
- Data retention supply voltage of 1.5 to 3.3 V
- Direct TTL compatibility for all inputs and outputs
- Wide operating temperature range of  $-40^\circ$  to  $85^\circ\text{C}$
- Standby Current (maximum):

3.3 V	10 $\mu$ A
3.0 V	5 $\mu$ A

- Access Times (maximum):

	TC55W800FT	
	-55	-70
Access Time	55 ns	70 ns
$\overline{\text{CE1}}$ Access Time	55 ns	70 ns
$\overline{\text{CE2}}$ Access Time	55 ns	70 ns
$\overline{\text{OE}}$ Access Time	30 ns	35 ns

- Package:  
TSOP 48-P-1220-0.50 (Weight: 0.52 g typ)

**PIN ASSIGNMENT (TOP VIEW)****48 PIN TSOP**

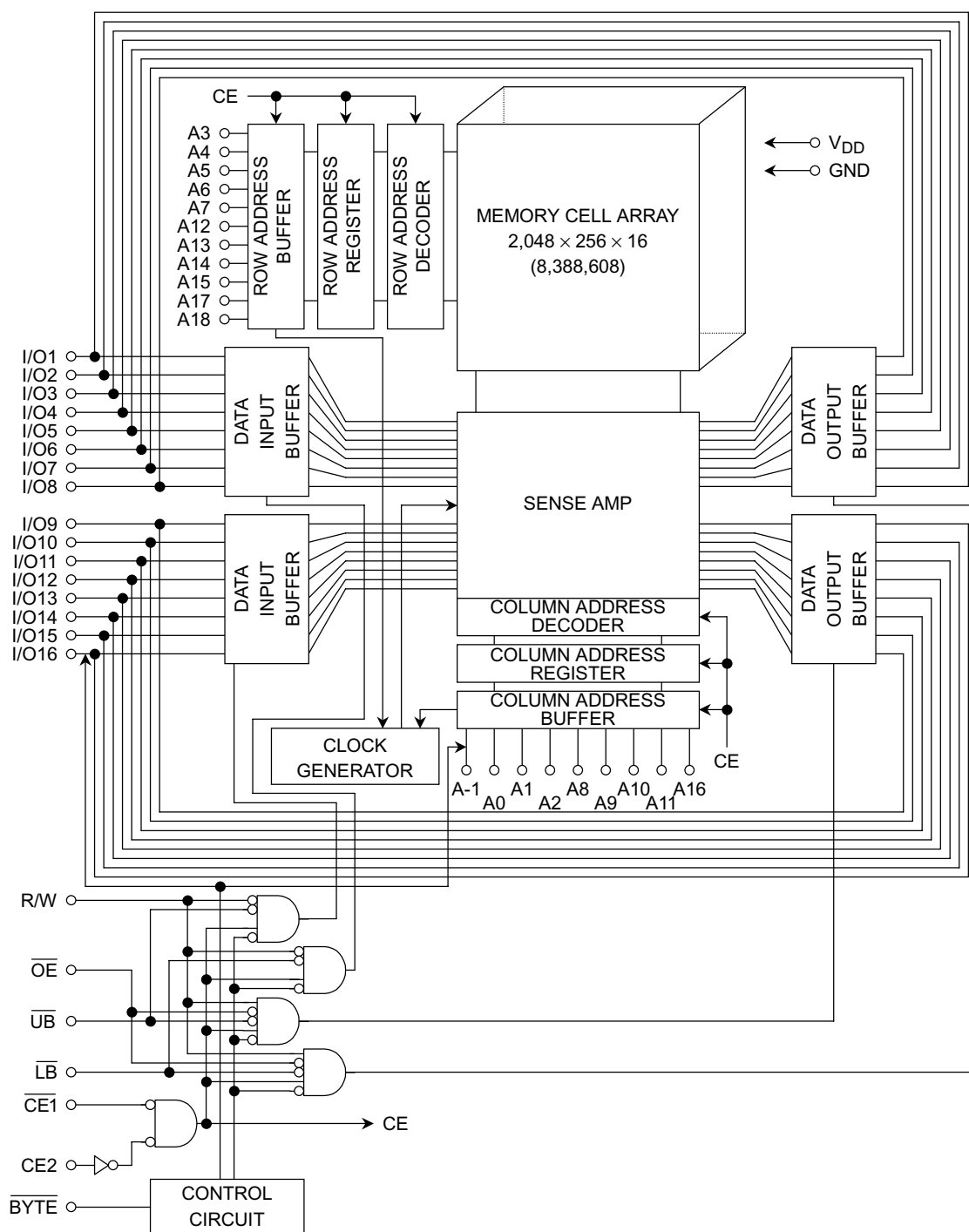
(Normal)

**PIN NAMES**

A0~A18	Address Inputs (Word Mode)
A-1~A18	Address Inputs (Byte Mode)
$\overline{\text{CE1}}$ , $\overline{\text{CE2}}$	Chip Enable
R/W	Read/Write Control
$\overline{\text{OE}}$	Output Enable
$\overline{\text{LB}}$ , $\overline{\text{UB}}$	Data Byte Control
I/O1~I/O16	Data Inputs/Outputs
BYTE	Byte ( $\times 8$ mode) Enable
$V_{DD}$	Power
GND	Ground
NC	No Connection

Pin No.	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
Pin Name	A15	A14	A13	A12	A11	A10	A9	A8	NC	NC	R/W	CE2	NC	$\overline{\text{UB}}$	$\overline{\text{LB}}$	A18
Pin No.	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32
Pin Name	A17	A7	A6	A5	A4	A3	A2	A1	A0	$\overline{\text{CE1}}$	GND	$\overline{\text{OE}}$	I/O1	I/O9	I/O2	I/O10
Pin No.	33	34	35	36	37	38	39	40	41	42	43	44	45	46	47	48
Pin Name	I/O3	I/O11	I/O4	I/O12	$V_{DD}$	I/O5	I/O13	I/O6	I/O14	I/O7	I/O15	I/O8	I/O16 /A-1	GND	$\overline{\text{BYTE}}$	A16

## BLOCK DIAGRAM



## OPERATING MODE

MODE	$\overline{CE1}$	CE2	$\overline{OE}$	R/W	BYTE	$\overline{LB}$	$\overline{UB}$	I/O1~I/O8	I/O9~I/O15	I/O16	POWER
Read	L	H	L	H	L	*	*	Output	High-Z	A-1	I <sub>DDO</sub>
	L	H	L	H	H	L	L	Output	Output	Output	I <sub>DDO</sub>
	L	H	L	H	H	H	L	High-Z	Output	Output	I <sub>DDO</sub>
	L	H	L	H	H	L	H	Output	High-Z	High-Z	I <sub>DDO</sub>
Write	L	H	*	L	L	*	*	Input	High-Z	A-1	I <sub>DDO</sub>
	L	H	*	L	H	L	L	Input	Input	Input	I <sub>DDO</sub>
	L	H	*	L	H	H	L	High-Z	Input	Input	I <sub>DDO</sub>
	L	H	*	L	H	L	H	Input	High-Z	High-Z	I <sub>DDO</sub>
Output Deselect	L	H	H	H	L	*	*	High-Z	High-Z	A-1	I <sub>DDO</sub>
	L	H	H	H	H	*	*	High-Z	High-Z	High-Z	I <sub>DDO</sub>
	L	H	L	H	H	H	H	High-Z	High-Z	High-Z	I <sub>DDO</sub>
Standby	H	*	*	*	H or L	*	*	High-Z	High-Z	High-Z	I <sub>DDS</sub>
	*	L	*	*	H or L	*	*	High-Z	High-Z	High-Z	I <sub>DDS</sub>

\* = don't care  
H = logic high  
L = logic low

## MAXIMUM RATINGS

SYMBOL	RATING	VALUE	UNIT
V <sub>DD</sub>	Power Supply Voltage	-0.3~4.2	V
V <sub>IN</sub>	Input Voltage	-0.3*~4.2	V
V <sub>I/O</sub>	Input/Output Voltage	-0.5~V <sub>DD</sub> + 0.5	V
P <sub>D</sub>	Power Dissipation	0.6	W
T <sub>solder</sub>	Soldering Temperature (10s)	260	°C
T <sub>stg</sub>	Storage Temperature	-55~150	°C
T <sub>opr</sub>	Operating Temperature	-40~85	°C

\*: -2.0 V when measured at a pulse width of 20ns

## DC RECOMMENDED OPERATING CONDITIONS (Ta = -40° to 85°C)

SYMBOL	PARAMETER		MIN	TYP	MAX	UNIT
V <sub>DD</sub>	Power Supply Voltage		2.3	—	3.3	V
V <sub>IH</sub>	Input High Voltage	V <sub>DD</sub> = 2.3 V~3.3 V	2.0	—	V <sub>DD</sub> + 0.3	V
		V <sub>DD</sub> = 2.7 V~3.3 V	2.2			
V <sub>IL</sub>	Input Low Voltage		-0.3*	—	V <sub>DD</sub> × 0.22	V
V <sub>DH</sub>	Data Retention Supply Voltage		1.5	—	3.3	V

\*: -2.0 V when measured at a pulse width of 20ns

**DC CHARACTERISTICS** ( $T_a = -40^\circ$  to  $85^\circ\text{C}$ ,  $V_{DD} = 2.3$  to  $3.3\text{ V}$ )

SYMBOL	PARAMETER	TEST CONDITION			MIN	TYP	MAX	UNIT
I <sub>IL</sub>	Input Leakage Current	V <sub>IN</sub> = 0 V~V <sub>DD</sub>			—	—	±1.0	μA
I <sub>OH</sub>	Output High Current	V <sub>OH</sub> = V <sub>DD</sub> − 0.5 V			−0.5	—	—	mA
I <sub>OL</sub>	Output Low Current	V <sub>OL</sub> = 0.4 V			2.1	—	—	mA
I <sub>LO</sub>	Output Leakage Current	CE1 = V <sub>IH</sub> or CE2 = V <sub>IL</sub> or R/W = V <sub>IL</sub> or OE = V <sub>IH</sub> , V <sub>OUT</sub> = 0 V~V <sub>DD</sub>			—	—	±1.0	μA
I <sub>DDO1</sub>	Operating Current	CE1 = V <sub>IL</sub> and CE2 = V <sub>IH</sub> and R/W = V <sub>IH</sub> , I <sub>OUT</sub> = 0 mA, Other Input = V <sub>IH</sub> /V <sub>IL</sub> , BYTE = V <sub>DD</sub> or 0 V	t <sub>cycle</sub>	55 ns	—	—	60	mA
				70 ns	—	—	50	
				1 μs	—	—	10	
I <sub>DDO2</sub>	Operating Current	CE1 = 0.2 V and CE2 = V <sub>DD</sub> − 0.2 V and R/W = V <sub>DD</sub> − 0.2 V, I <sub>OUT</sub> = 0 mA, Other Input = V <sub>DD</sub> − 0.2 V/0.2 V, BYTE = V <sub>DD</sub> or 0 V	t <sub>cycle</sub>	55 ns	—	—	55	mA
				70 ns	—	—	45	
				1 μs	—	—	5	
I <sub>DDS1</sub>	Standby Current	CE1 = V <sub>IH</sub> or CE2 = V <sub>IL</sub> , BYTE = V <sub>DD</sub> or 0 V			—	—	2	mA
I <sub>DDS2</sub> (Note)		CE1 = V <sub>DD</sub> − 0.2 V or CE2 = 0.2 V, V <sub>DD</sub> = 1.5 V~3.3 V, BYTE = V <sub>DD</sub> or 0 V	V <sub>DD</sub> = 3.0 V ± 10%	Ta = 25°C	—	—	1	μA
				Ta = −40~85°C	—	—	10	
			V <sub>DD</sub> = 3.0 V	Ta = 25°C	—	0.05	0.5	
				Ta = −40~40°C	—	—	1	
	Ta = −40~85°C	—	—	5				

Note: In standby mode with  $\overline{CE1} \geq V_{DD} - 0.2\text{ V}$ , these limits are assured for the condition  $CE2 \geq V_{DD} - 0.2\text{ V}$  or  $CE2 \leq 0.2\text{ V}$ .

**CAPACITANCE** ( $T_a = 25^\circ\text{C}$ ,  $f = 1\text{ MHz}$ )

SYMBOL	PARAMETER	TEST CONDITION	MAX	UNIT
$C_{IN}$	Input Capacitance	$V_{IN} = \text{GND}$	10	pF
$C_{OUT}$	Output Capacitance	$V_{OUT} = \text{GND}$	10	pF

Note: This parameter is periodically sampled and is not 100% tested.

**AC CHARACTERISTICS AND OPERATING CONDITIONS**(Ta = -40° to 85°C, V<sub>DD</sub> = 2.7 to 3.3 V)**READ CYCLE**

SYMBOL	PARAMETER	TC55W800FT				UNIT
		-55		-70		
		MIN	MAX	MIN	MAX	
t <sub>RC</sub>	Read Cycle Time	55	—	70	—	ns
t <sub>ACC</sub>	Address Access Time	—	55	—	70	
t <sub>CO1</sub>	Chip Enable( $\overline{CE1}$ ) Access Time	—	55	—	70	
t <sub>CO2</sub>	Chip Enable(CE2) Access Time	—	55	—	70	
t <sub>OE</sub>	Output Enable Access Time	—	30	—	35	
t <sub>BA</sub>	Data Byte Control Access Time	—	30	—	35	
t <sub>COE</sub>	Chip Enable Low to Output Active	5	—	5	—	
t <sub>OEE</sub>	Output Enable Low to Output Active	0	—	0	—	
t <sub>BE</sub>	Data Byte Control Low to Output Active	0	—	0	—	
t <sub>OD</sub>	Chip Enable High to Output High-Z	—	25	—	30	
t <sub>ODO</sub>	Output Enable High to Output High-Z	—	25	—	30	
t <sub>BD</sub>	Data Byte Control High to Output High-Z	—	25	—	30	
t <sub>OH</sub>	Output Data Hold Time	10	—	10	—	

**WRITE CYCLE**

SYMBOL	PARAMETER	TC55W800FT				UNIT
		-55		-70		
		MIN	MAX	MIN	MAX	
t <sub>WC</sub>	Write Cycle Time	55	—	70	—	ns
t <sub>WP</sub>	Write Pulse Width	45	—	50	—	
t <sub>CW</sub>	Chip Enable to End of Write	50	—	60	—	
t <sub>BW</sub>	Data Byte Control to End of Write	45	—	50	—	
t <sub>AS</sub>	Address Setup Time	0	—	0	—	
t <sub>WR</sub>	Write Recovery Time	0	—	0	—	
t <sub>ODW</sub>	R/W Low to Output High-Z	—	25	—	30	
t <sub>OEW</sub>	R/W High to Output Active	0	—	0	—	
t <sub>DS</sub>	Data Setup Time	25	—	30	—	
t <sub>DH</sub>	Data Hold Time	0	—	0	—	

**AC TEST CONDITIONS**

PARAMETER	TEST CONDITION
Output load	30 pF + 1 TTL Gate
Input pulse level	0.4 V, 2.4 V
Timing measurements	V <sub>DD</sub> × 0.5
Reference level	V <sub>DD</sub> × 0.5
t <sub>R</sub> , t <sub>F</sub>	5 ns

## AC CHARACTERISTICS AND OPERATING CONDITIONS

(Ta = -40° to 85°C, V<sub>DD</sub> = 2.3 to 3.3 V)

### READ CYCLE

SYMBOL	PARAMETER	TC55W800FT				UNIT
		-55		-70		
		MIN	MAX	MIN	MAX	
t <sub>RC</sub>	Read Cycle Time	70	—	85	—	ns
t <sub>ACC</sub>	Address Access Time	—	70	—	85	
t <sub>CO1</sub>	Chip Enable( $\overline{CE1}$ ) Access Time	—	70	—	85	
t <sub>CO2</sub>	Chip Enable(CE2) Access Time	—	70	—	85	
t <sub>OE</sub>	Output Enable Access Time	—	35	—	45	
t <sub>BA</sub>	Data Byte Control Access Time	—	35	—	45	
t <sub>COE</sub>	Chip Enable Low to Output Active	5	—	5	—	
t <sub>OEE</sub>	Output Enable Low to Output Active	0	—	0	—	
t <sub>BE</sub>	Data Byte Control Low to Output Active	0	—	0	—	
t <sub>OD</sub>	Chip Enable High to Output High-Z	—	30	—	35	
t <sub>ODO</sub>	Output Enable High to Output High-Z	—	30	—	35	
t <sub>BD</sub>	Data Byte Control High to Output High-Z	—	30	—	35	
t <sub>OH</sub>	Output Data Hold Time	10	—	10	—	

### WRITE CYCLE

SYMBOL	PARAMETER	TC55W800FT				UNIT
		-55		-70		
		MIN	MAX	MIN	MAX	
t <sub>WC</sub>	Write Cycle Time	70	—	85	—	ns
t <sub>WP</sub>	Write Pulse Width	50	—	55	—	
t <sub>CW</sub>	Chip Enable to End of Write	60	—	70	—	
t <sub>BW</sub>	Data Byte Control to End of Write	50	—	55	—	
t <sub>AS</sub>	Address Setup Time	0	—	0	—	
t <sub>WR</sub>	Write Recovery Time	0	—	0	—	
t <sub>ODW</sub>	R/W Low to Output High-Z	—	30	—	35	
t <sub>OEW</sub>	R/W High to Output Active	0	—	0	—	
t <sub>DS</sub>	Data Setup Time	30	—	35	—	
t <sub>DH</sub>	Data Hold Time	0	—	0	—	

## AC TEST CONDITIONS

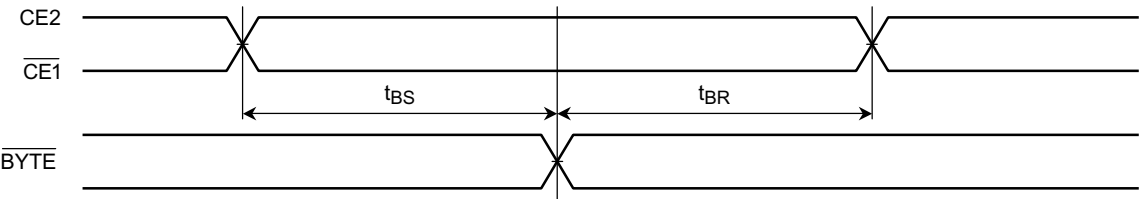
PARAMETER	TEST CONDITION
Output load	30 pF + 1 TTL Gate
Input pulse level	V <sub>DD</sub> - 0.2 V, 0.2 V
Timing measurements	V <sub>DD</sub> × 0.5
Reference level	V <sub>DD</sub> × 0.5
t <sub>R</sub> , t <sub>F</sub>	5 ns

BYTE FUNCTION

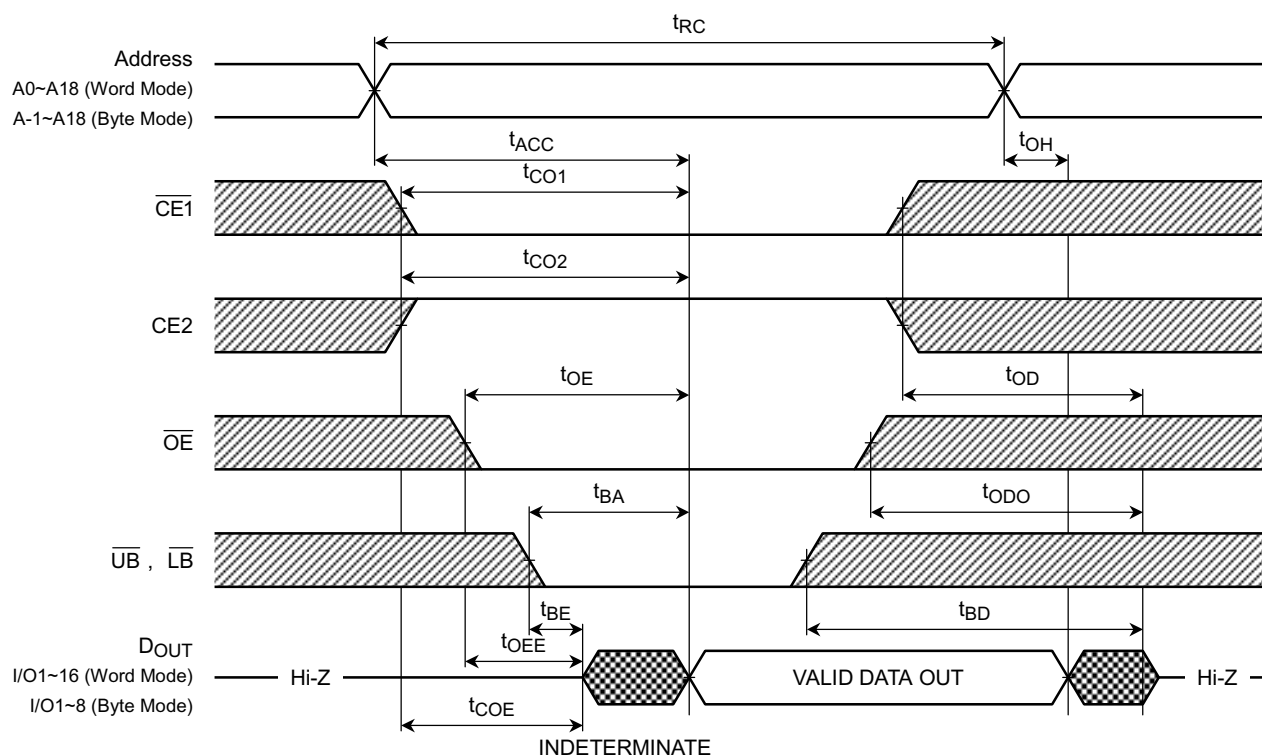
SYMBOL	PARAMETER	MIN	MAX	UNIT
t <sub>BS</sub>	$\overline{\text{BYTE}}$ Setup Time	5	—	ms
t <sub>BR</sub>	$\overline{\text{BYTE}}$ Recovery Time	5	—	ms

TIMING DIAGRAMS

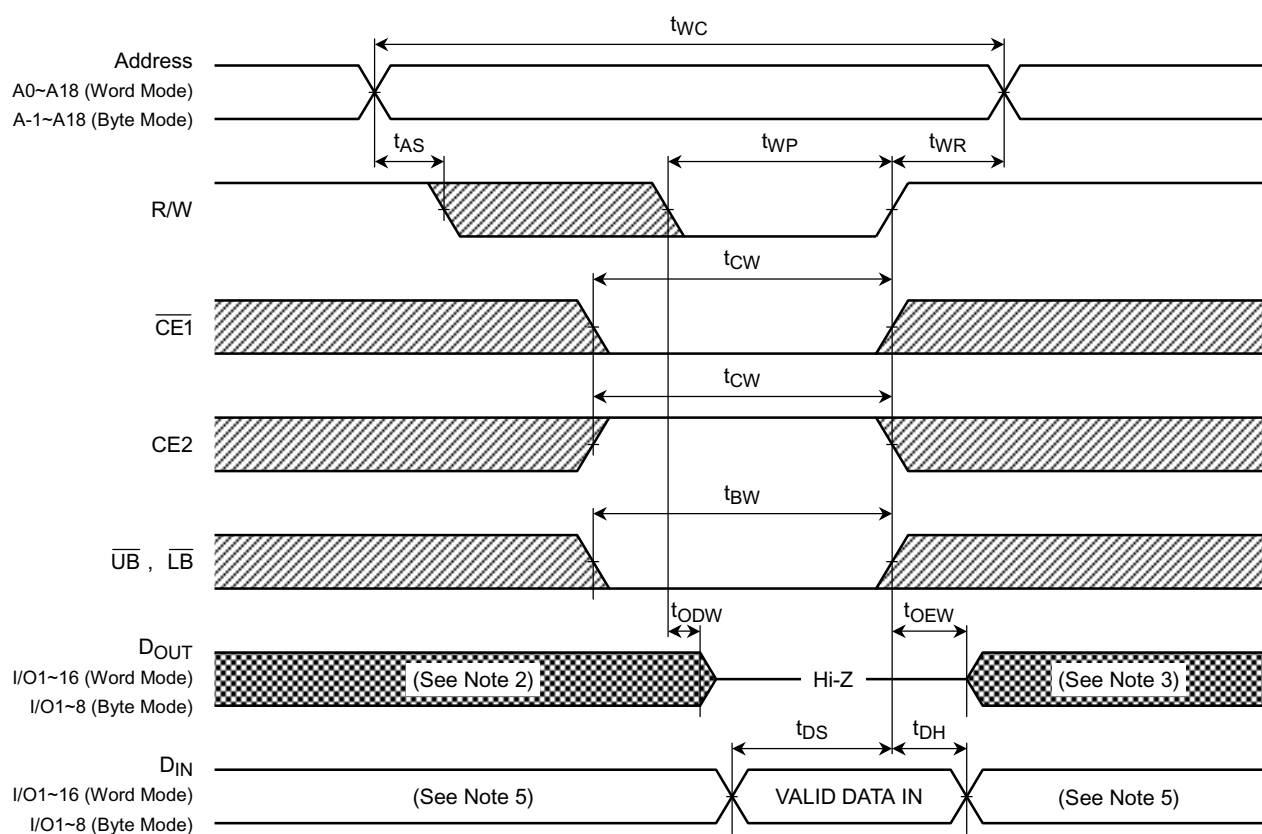
$\overline{\text{BYTE}}$



READ CYCLE (See Note 1)

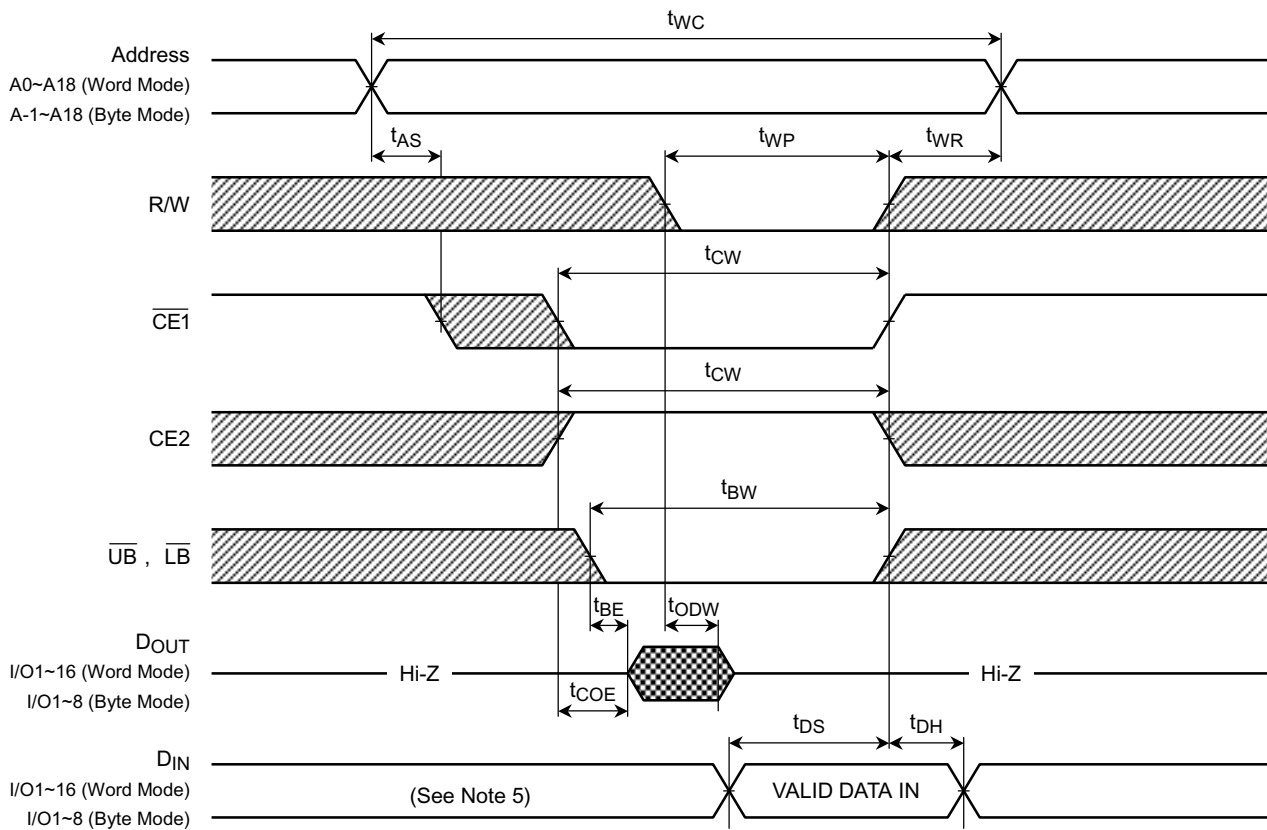


WRITE CYCLE 1 (R/W CONTROLLED) (See Note 4)

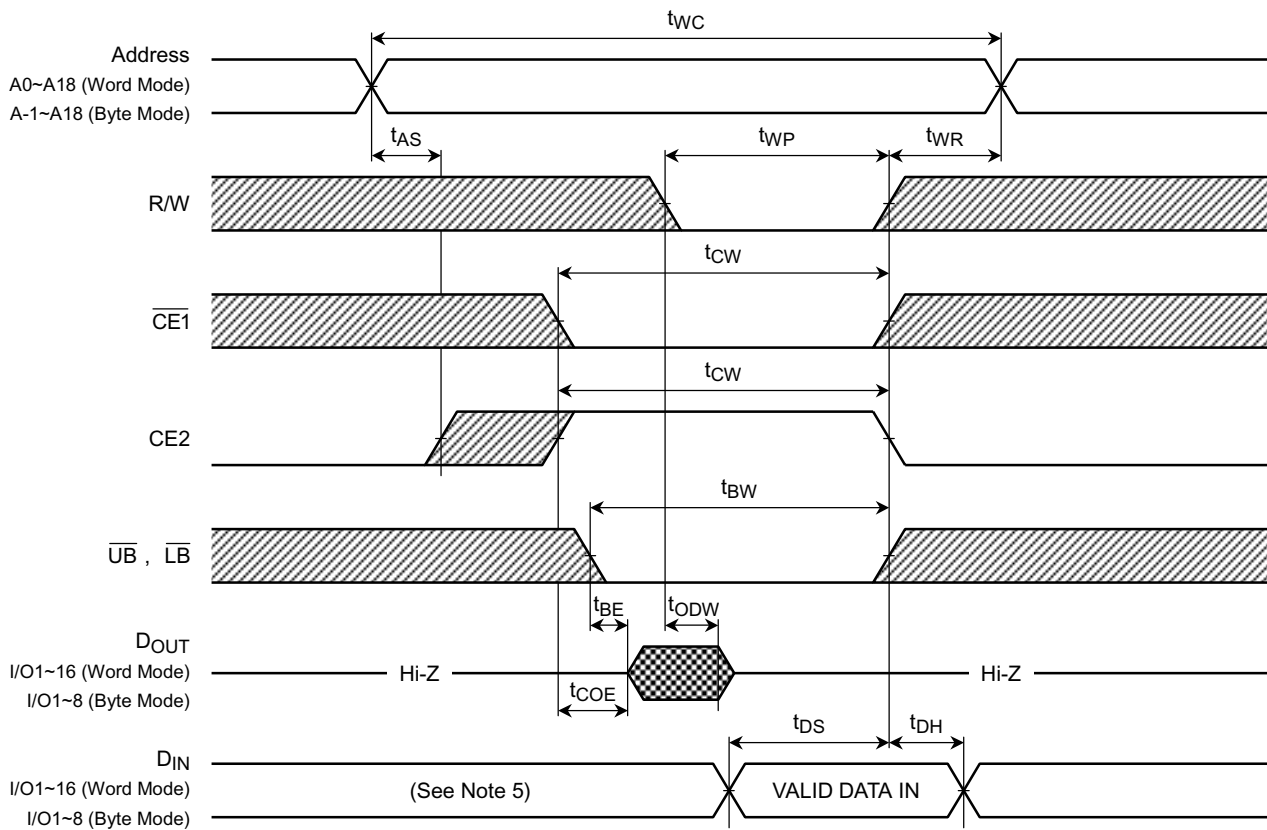


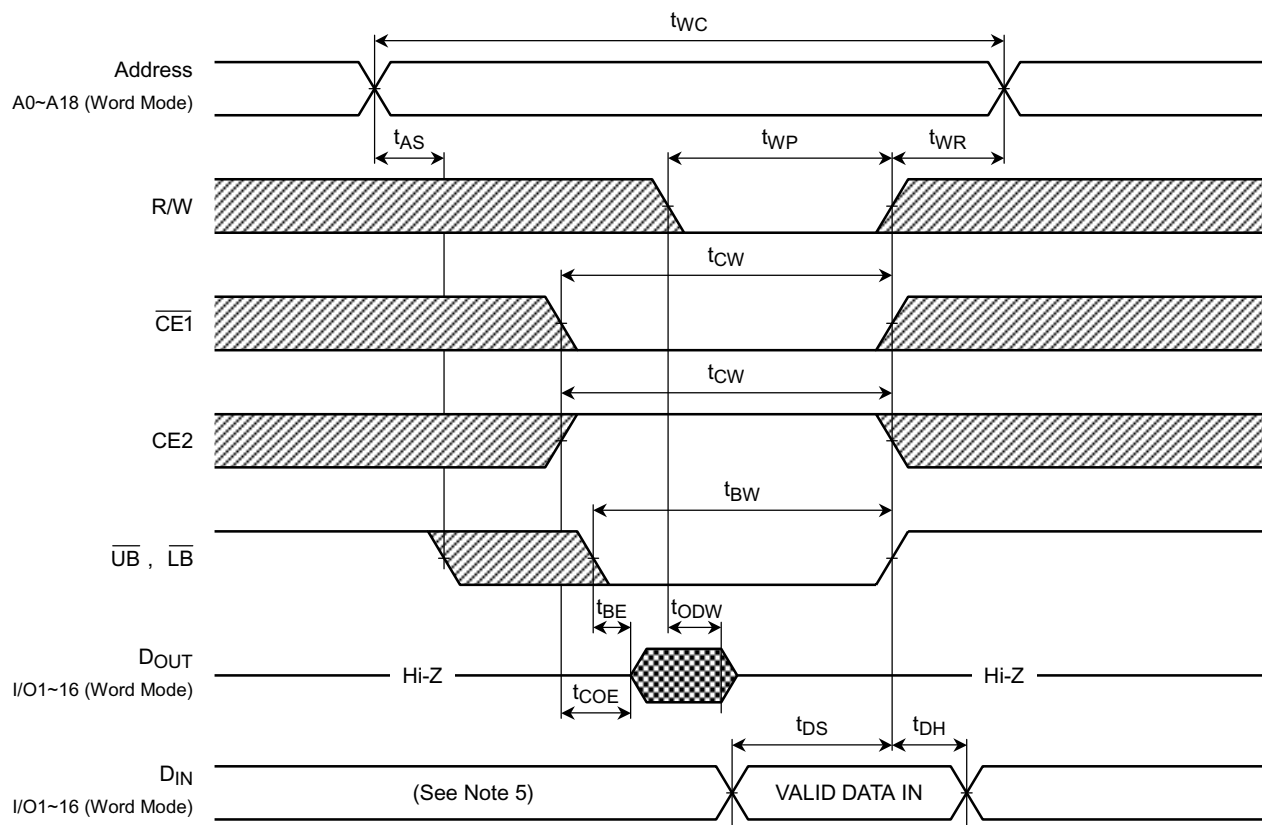


## WRITE CYCLE 2 ( $\overline{\text{CE1}}$ CONTROLLED) (See Note 4)



## WRITE CYCLE 3 ( $\text{CE2}$ CONTROLLED) (See Note 4)



**WRITE CYCLE 4 ( $\overline{\text{UB}}$ ,  $\overline{\text{LB}}$  CONTROLLED)** (See Note 4)

**Note:**

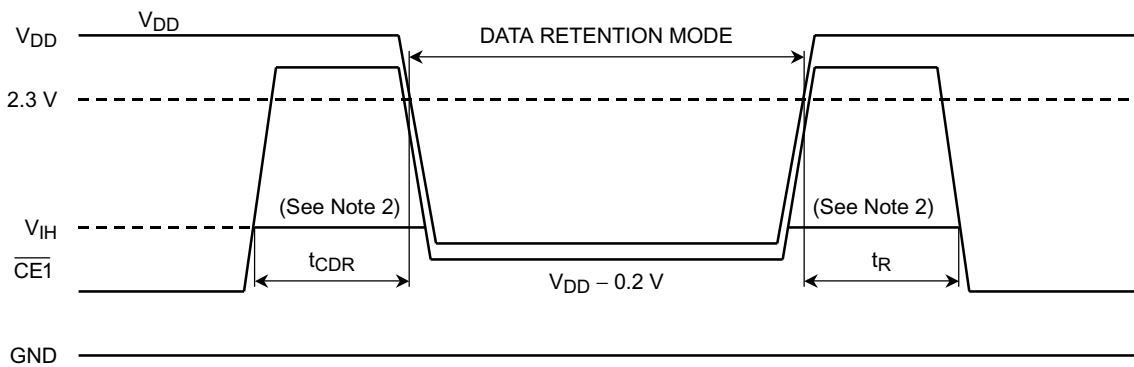
- (1) R/W remains HIGH for the read cycle.
- (2) If  $\overline{\text{CE1}}$  goes LOW(or CE2 goes HIGH) coincident with or after R/W goes LOW, the outputs will remain at high impedance.
- (3) If  $\overline{\text{CE1}}$  goes HIGH(or CE2 goes LOW) coincident with or before R/W goes HIGH, the outputs will remain at high impedance.
- (4) If  $\overline{\text{OE}}$  is HIGH during the write cycle, the outputs will remain at high impedance.
- (5) Because I/O signals may be in the output state at this time, input signals of reverse polarity must not be applied.

**DATA RETENTION CHARACTERISTICS (Ta = -40° to 85°C)**

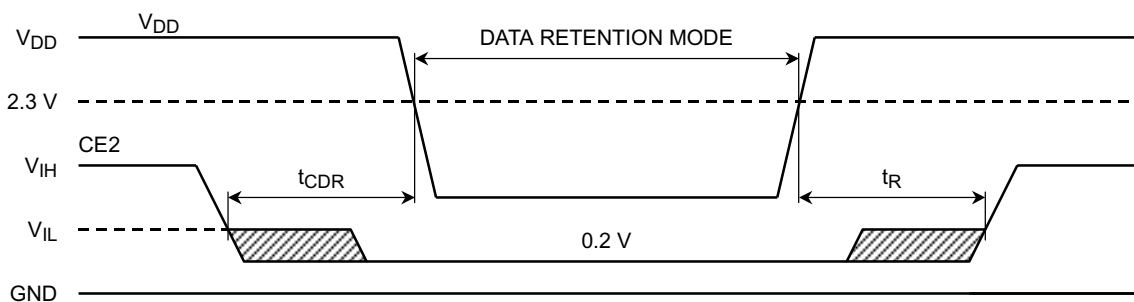
SYMBOL	PARAMETER			MIN	TYP	MAX	UNIT
V <sub>DH</sub>	Data Retention Supply Voltage			1.5	—	3.3	V
I <sub>DDS2</sub>	Standby Current	V <sub>DH</sub> = 3.3 V	Ta = −40~85°C	—	—	10	μA
		V <sub>DH</sub> = 3.0 V	Ta = −40~40°C	—	—	1	
			Ta = −40~85°C	—	—	5	
t <sub>CDR</sub>	Chip Deselect to Data Retention Mode Time			0	—	—	ns
t <sub>R</sub>	Recovery Time			t <sub>RC</sub> <sup>(See Note)</sup>	—	—	ns

Note: Read cycle time

**CE1 CONTROLLED DATA RETENTION MODE** (See Note 1)



**CE2 CONTROLLED DATA RETENTION MODE** (See Note 3)



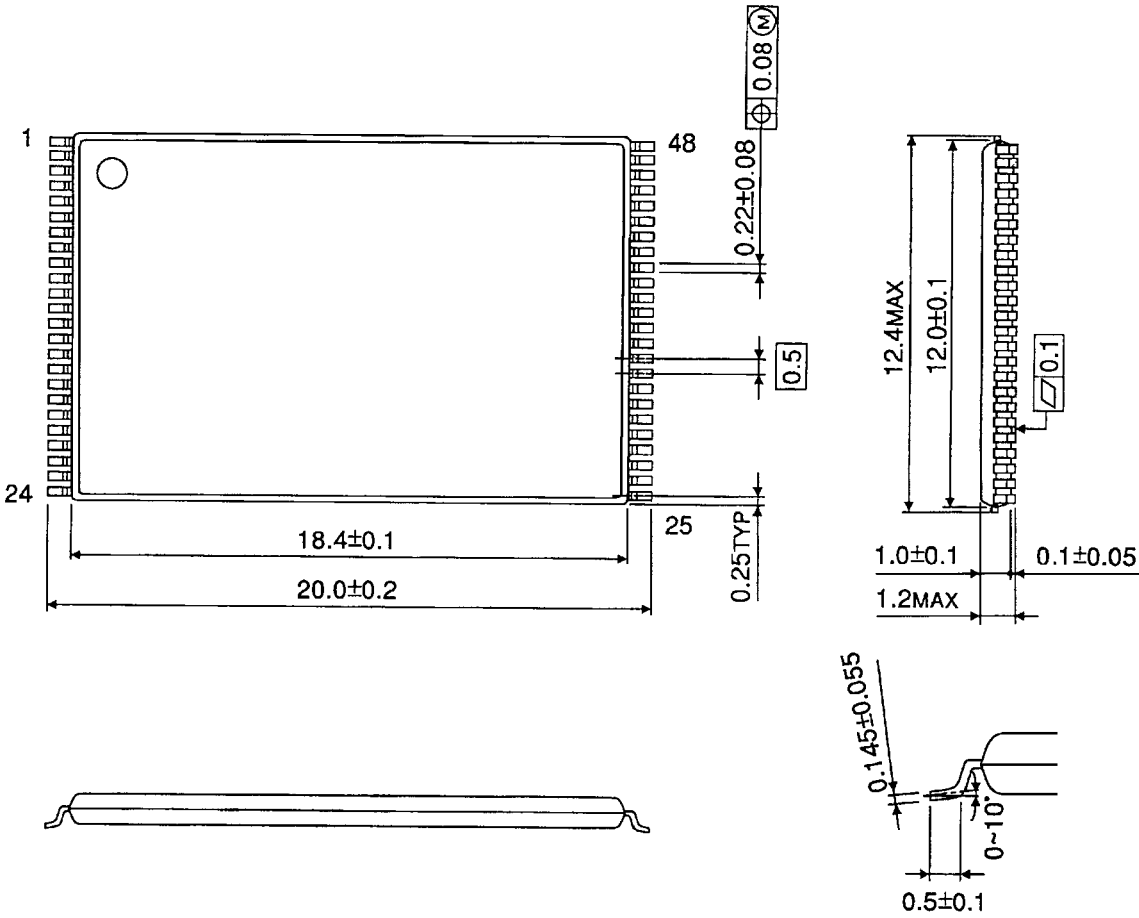
Note:

- (1) In  $\overline{\text{CE1}}$  controlled data retention mode, minimum standby current mode is entered when  $\text{CE2} \leq 0.2 \text{ V}$  or  $\text{CE2} \geq V_{\text{DD}} - 0.2 \text{ V}$ .
- (2) When  $\overline{\text{CE1}}$  is operating at the V<sub>IH</sub> level, the operating current is given by I<sub>DDS1</sub> during the transition of V<sub>DD</sub> from 2.3 to 2.2V.
- (3) In CE2 controlled data retention mode, minimum standby current mode is entered when  $\text{CE2} \leq 0.2 \text{ V}$ .

PACKAGE DIMENSIONS

TSOP I 48-P-1220-0.50

Unit : mm



Weight: 0.52 g (typ)

**RESTRICTIONS ON PRODUCT USE**

000707EBA

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