

748MHz VCO

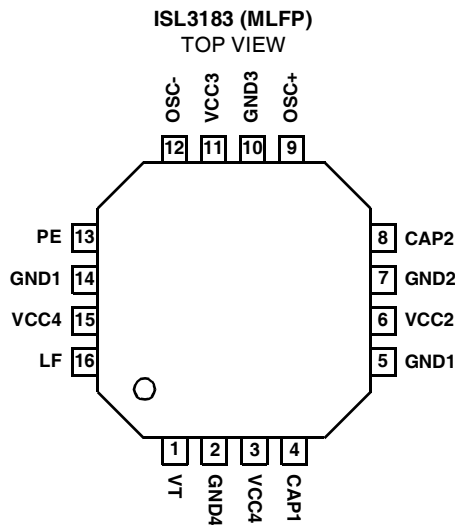


The ISL3183 is a 748MHz monolithic VCO designed to simplify and reduce the cost and size of the VCO function for PRISM® WLAN applications.

This fully integrated VCO does not require external elements such as inductors and varactors. Load pull rejection is excellent, eliminating the need for an external buffer amplifier. A differential design provides inherent rejection of spurious signals which simplifies the PCB layout.

The ISL3183 is housed in a 16 lead MLFP package well suited for PCMCIA board applications.

Pinout



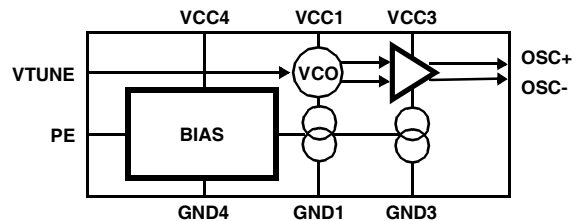
Features

- Single Supply 2.7V to 3.0V
- Frequency 748MHz
- Fully integrated / No External Varactors or Resonators Required
- High Isolation Output Buffer / Reduced Load Pulling
- Differential Design / Reduced Spurs
- Digitally Controlled Power Down Mode

Applications

- Systems Targeting IEEE802.11b, 11Mbps Standard
- Wireless Local Area Networks
- PCMCIA Wireless Transceivers
- TDMA Packet Protocol Radios

Simplified Block Diagram



Ordering Information

PART NUMBER	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
ISL3183IR	-40 to 85	16 Ld MLFP	L16.4x4
ISL3183IR96	-40 to 85	Tape and Reel	

Pin Descriptions

PIN NUMBER	NAME	DESCRIPTION
1	VT	Tuning Voltage.
2	GND4	DC and RF Ground.
3	VCC4	Power Supply.
4	CAP1	Bypass Capacitor 1.
5	GND1	DC and RF Ground.
6	VCC2	Power Supply.
7	GND2	DC and RF Ground.
8	CAP2	Bypass Capacitor 2.
9	OSC+	VCO Output +.
10	GND3	DC and RF Ground.
11	VCC3	Power Supply.
12	OSC-	VCO Output -.
13	PE	Digital input control pin to enable operation of the Power Amplifier. Enable logic level is high.
14	GND1	DC and RF Ground.
15	VCC1	Power Supply.
16	LF	Low Pass Filtering.

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Absolute Maximum Ratings

Supply Voltage	3.6V
Voltage on Any Other Pin	-0.3 to V _{CC} +0.3V
V _{CC} to V _{CC} Decouple	-0.3 to +0.3V
Any GND to GND	-0.3 to +0.3V

Thermal Information

Thermal Resistance (Typical, Note 1)	θ_{JA} (°C/W)
MLFP Package	42
Maximum Junction Temperature (Plastic Package)	150°C
Maximum Storage Temperature Range	-65°C to 150°C
Maximum Lead Temperature (Soldering 10s)	300°C

Operating Conditions

Temperature Range	-40 to 85°C
Supply Voltage Range	2.7V to 3.0V

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

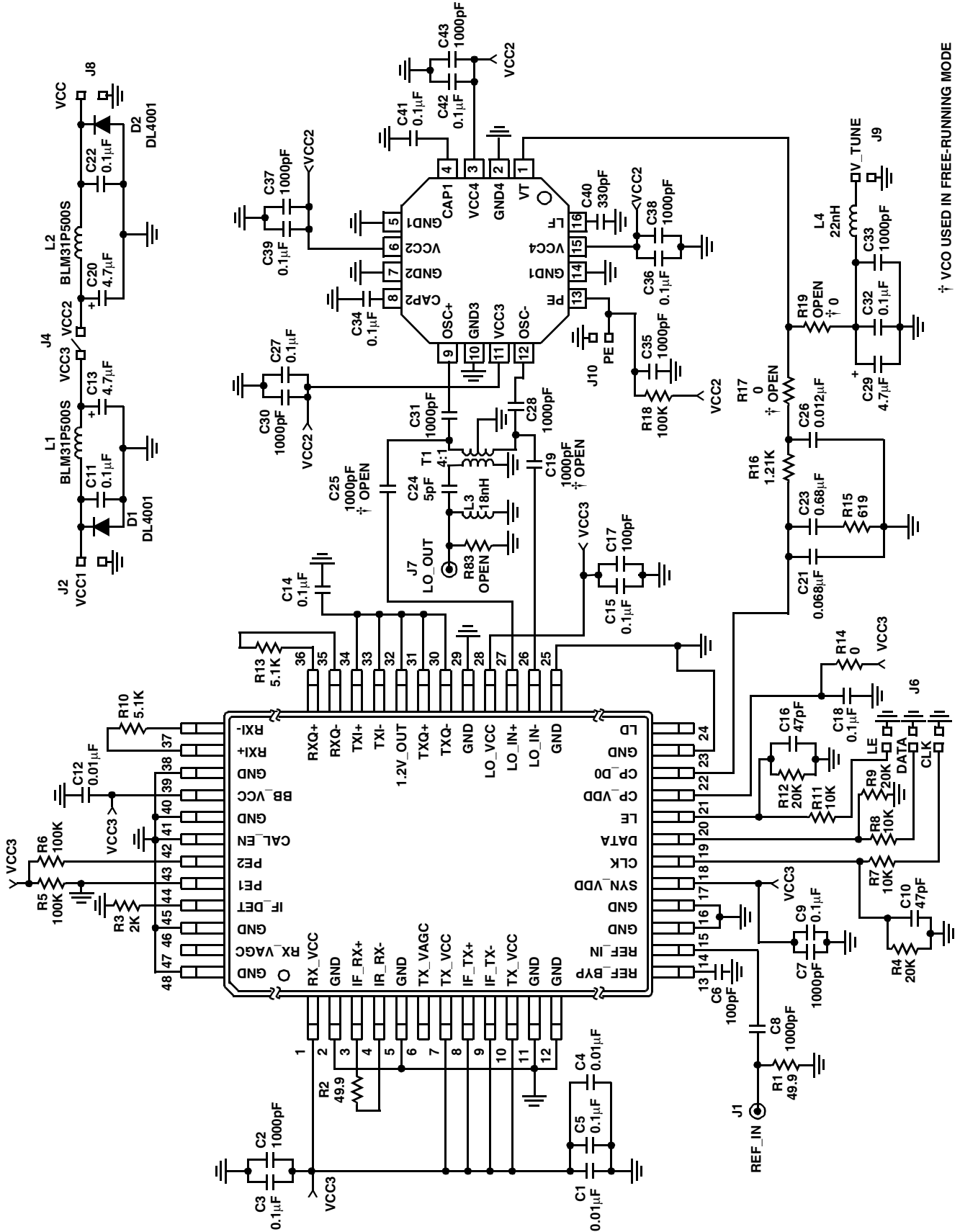
- θ_{JA} is measured in free air with the component mounted on a high effective thermal conductivity test board with "direct attach" features. See Tech Brief TB379.

General DC Electrical Specifications V_{CC} = 2.85V

PARAMETER	TEMP. (°C)	MIN	TYP	MAX	UNITS
Supply Voltage	25	2.7	2.85	3.0	V
Supply Current	25	-	8.9	12	mA
Power Down Supply Current	25	-	-	180	µA
Power Up Time	25	-	1000	-	µs
Power Down Time	25	-	300	-	µs
CMOS Low Level Input Voltage	25	-	-	0.3*V _{DD}	V
CMOS High Level Input Voltage	25	0.7*V _{DD}	-	-	V

VCO AC Electrical Specifications V_{CC} = 2.85V, ISL3183EVAL used as a platform, Unless Otherwise Specified

PARAMETER	TEST CONDITIONS	TEMP. (°C)	MIN	TYP	MAX	UNITS
RF Frequency Range		25	738	-	755	MHz
Tuning Voltage		25	0.5	1.2	2.2	V
VCO Gain		Full	-	33	-	MHz/V
Phase Noise	Offset 10kHz	25	-	-78	-	dBc/Hz
Harmonic Outputs		Full	-	-20	-	dBc
Output Power	Calibrated for Losses on the Board	25	-18.8	-16	-10	dBm
Supply Pushing	V _{CC} = 2.7V - 3V	25	-0.2	-	0.2	MHz
Load Pulling	VSWR = 2:1 (NOTE: Limits are Based on Characterization)	Full	-0.2	-	0.2	MHz
Load Impedance		Full	-	300	-	Ohms
Output VSWR	(NOTE: Limits are Based on Characterization)	Full	-	-	2.2:1	-



† VCO USED IN FREE-RUNNING MODE

FIGURE 1. ISL3183EVAL BOARD SCHEMATIC

Typical Performance Curves

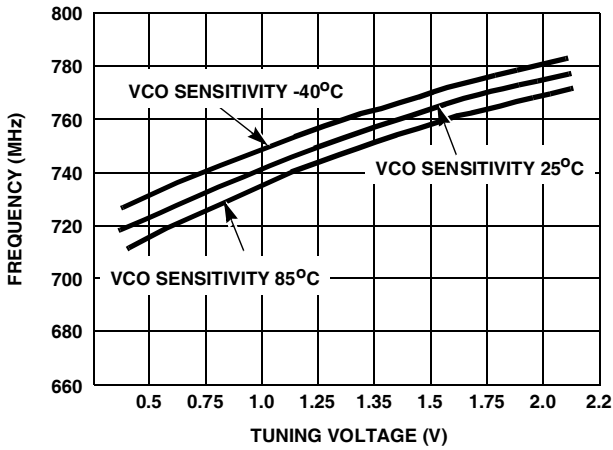


FIGURE 2. TYPICAL VCO SENSITIVITY (FR. OVER VT)

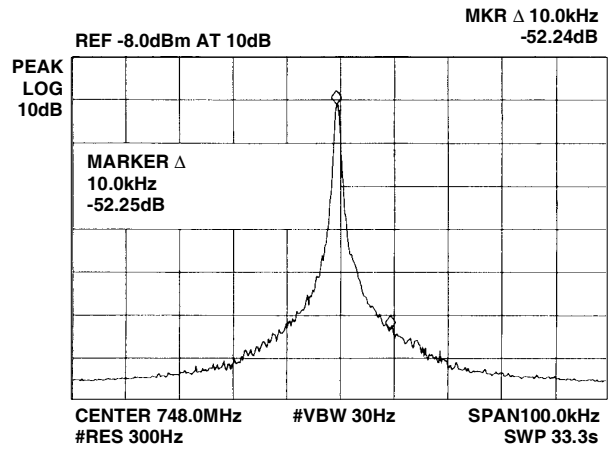


FIGURE 3. TYPICAL EVAL BOARD PHASE NOISE

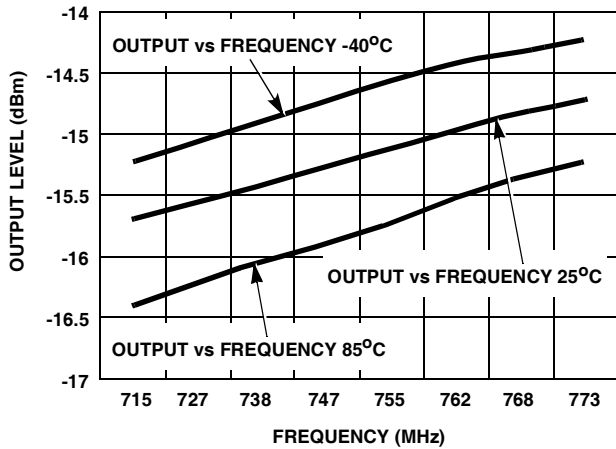


FIGURE 4. TYPICAL EVAL BOARD OUTPUT POWER vs FREQUENCY

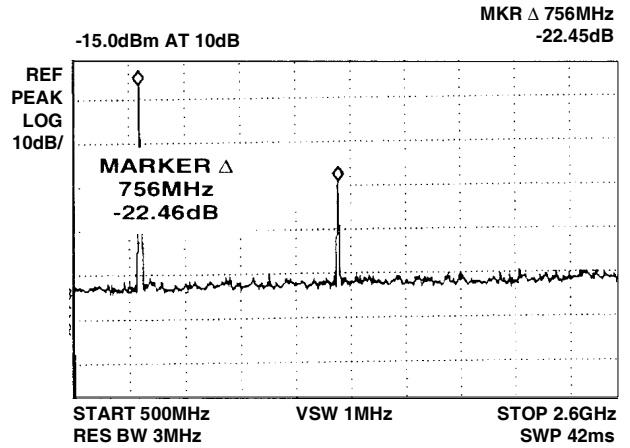


FIGURE 5. TYPICAL EVAL BOARD HARMONIC OUTPUTS

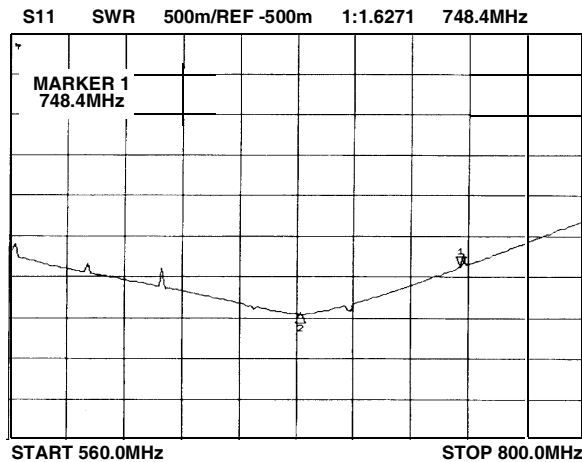
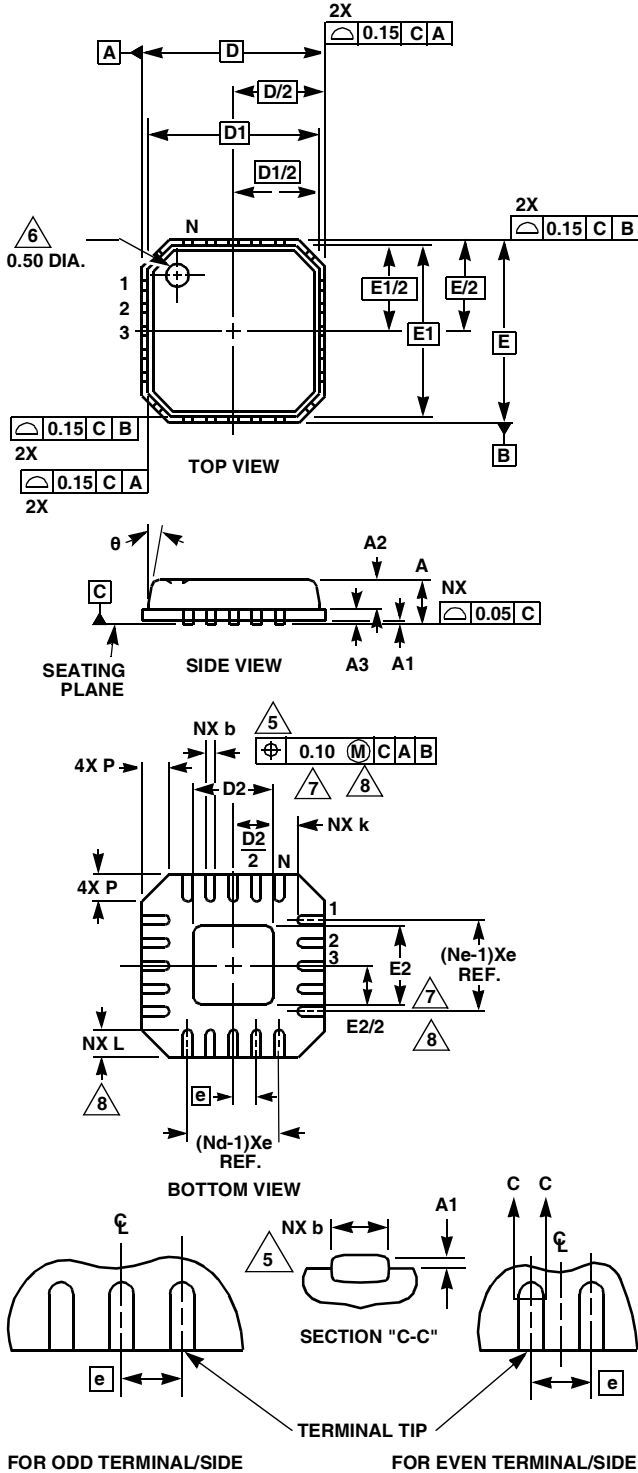


FIGURE 6. TYPICAL EVAL BOARD VSWR

Micro Lead Frame Plastic Package (MLFP)



L16.4x4
16 LEAD MICRO LEAD FRAME PLASTIC PACKAGE
(COMPLIANT TO JEDEC MO-220-VGGC ISSUE C)

SYMBOL	MILLIMETERS			NOTES
	MIN	NOMINAL	MAX	
A	-	-	0.90	-
A1	-	-	0.05	-
A2	-	-	0.70	-
A3	0.20 REF			-
b	0.23	0.28	0.35	5,8
D	4.00 BSC			-
D1	3.75 BSC			-
D2	1.95	2.10	2.25	7,8
E	4.00 BSC			-
E1	3.75 BSC			-
E2	1.95	2.10	2.25	7,8
e	0.65 BSC			-
k	0.25	-	-	-
L	0.50	0.60	0.75	8
N	16			2
Nd	4			3
Ne	4			3
P	-	-	0.60	-
θ	-	-	12	-

Rev. 3 6/01

NOTES:

1. Dimensioning and tolerancing per ASME Y14.5-1994.
2. N is the number of terminals.
3. Nd is the number of terminals in the X direction, and Ne is the number of terminals in the Y direction.
4. Controlling dimension: Millimeters. Converted dimensions to inches are not necessarily exact. Angles are in degrees.
5. Dimension b applies to the plated terminal and is measured between 0.20mm and 0.25mm from the terminal tip.
6. The Pin #1 identifier exists on the top surface as an indentation mark in the molded body.
7. Dimensions D2 and E2 are the maximum exposed pad dimensions for improved grounding and thermal performance.
8. Nominal dimensions provided to assist with PCB Land Pattern Design efforts, see Technical Brief TB389.

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