Preliminary

Features

512Kx24 bit CMOS Static

DSP Memory Solution

- Motorola DSP 5630x
- Analog Devices SHARC™

Random Access Memory Array

- Fast Access Times: 12, 15, 17, and 20ns
- Individual Byte Enables
- User Configurable Organization with Minimal Additional Logic
- Master Output Enable and Write Control
- TTL Compatible Inputs and Outputs
- Fully Static, No Clocks

Surface Mount Package

- 68 Lead PLCC, No. 99 JEDEC M0-47AE
- Small Footprint, 0.990 Sq. In.
- Multiple Ground Pins for Maximum Noise Immunity

Single +3.3V (±5%) Supply Operation

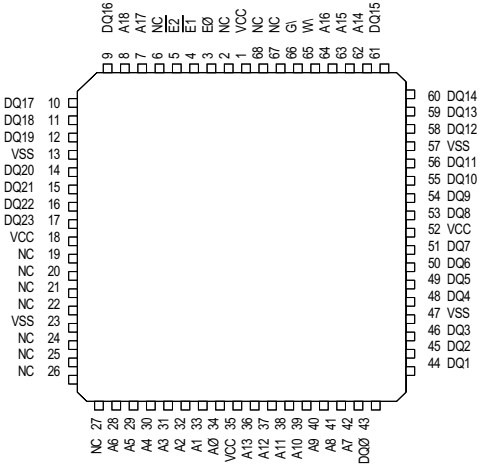
512Kx24 CMOS High Speed Static RAM

The EDI8L24512V is a high speed, 3.3V, 12 megabit SRAM. The device is available with access times of 12, 15,17 and 20ns allowing the creation of no wait state DSP memory solutions. The high speed, 3.3V supply voltage and control lines make the device ideal for creating fixed point DSP memory solutions.The device can used to create a single chip 512K x 24 external data memory solution for Motorola's DSP5630x (figure 3). Up to three 512K x 24 devices can be used with one DSP5630x, one for X data memory, one for Y data memory and one for Program memory (figure 4).

Alternatively a 512K x 48 program memory array for Analog's SHARC DSP can be created using two devices (figure 5). If this memory is too deep two 128K x 24s (EDI8L24128V) can be used to create a 128K x 48 array.

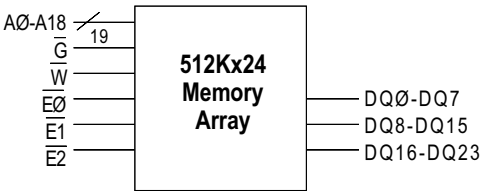
Note: Solder Reflow Temperature should not exceed 260°C for 10 seconds.

Pin Configurations and Block Diagram



Pin Names

AØ-A18	Address Inputs
$\overline{E}Ø$-$\overline{E}2$	Chip Enables (One per Byte)
$\overline{W}$	Master Write Enable
$\overline{G}$	Master Output Enable
DQØ-DQ23	Common Data Input/Output
VCC	Power (+3.3V±5%)
VSS	Ground
NC	No Connection



Absolute Maximum Ratings*

Voltage on any pin relative to VSS	-0.5V to 4.5V
Operating Temperature TA (Ambient)	
Commercial	0°C to + 70°C
Industrial	-40°C to +85°C
Storage Temperature	-55°C to +125°C
Power Dissipation	2.0 Watts
Output Current.	20 mA
Junction Temperature, TJ	175°C

*Stress greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions greater than those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Recommended DC Operating Conditions

Parameter	Sym	Min	Typ	Max	Units
Supply Voltage	VCC	3.135	3.3	3.465	V
Supply Voltage	VSS	0	0	0	V
Input High Voltage	VIH	2.2	--	VCC+0.3	V
Input Low Voltage	VIL	-0.3	--	0.8	V

AC Test Conditions

Input Pulse Levels	VSS to 3.0V
Input Rise and Fall Times	5ns
Input and Output Timing Levels	1.5V
Output Load	Figure 1

(note: For TEHQZ,TGHQZ and TWLQZ, CL = 5pF)

Figure 1

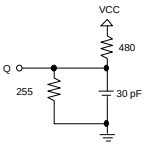
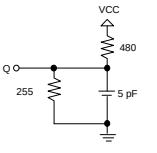


Figure 2



DC Electrical Characteristics

Parameter	Sym	Conditions	Min	Max 12/15	Max 17/20	Units mA
Operating Power Supply Current	ICC1	$\overline{W}$= VIL, II/O = 0mA, Min Cycle		540	480	mA
Standby (TTL) Supply Current	ICC2	$\overline{E} \geq$ VIH, VIN≤ VIL or VIN ≥ VIH, f=ØMHz		150	150	mA
Full Standby CMOS Supply Current	ICC3	$\overline{E} \geq$ VCC-0.2V VIN ≥ VCC-0.2V or VIN - 0.2V		30	30	mA
Input Leakage Current	ILI	VIN = 0V to VCC		±10		µA
Output Leakage Current	ILO	V I/O = 0V to VCC		±10		µA
Output High Volltage	VOH	IOH = -4.0mA	2.4			V
Output Low Voltage	VOL	IOL = 8.0mA		0.4		V

Truth Table

$\overline{G}$	$\overline{E}$	$\overline{W}$	Mode	Output	Power
X	H	X	Standby	High Z	ICC2 ICC3
H	L	H	Output Deselect	High Z	ICC1
L	L	H	Read	DOUT	ICC1
X	L	L	Write	DIN	ICC1

Capacitance

(f=1.0MHz, VIN=VCC or VSS)

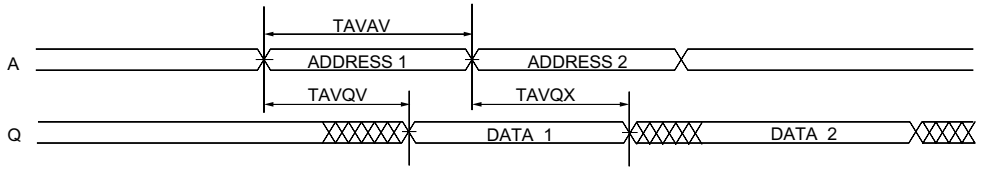
Parameter	Sym	Max	Unit
Address Lines	CI	30	pF
Data Lines	CD/Q	10	pF
Write & Output Enable Lines	$\overline{W}$, $\overline{G}$	30	pF
Chip Enable Lines	$\overline{E}$Ø-$\overline{E}$3	8	pF

AC Characteristics Read Cycle

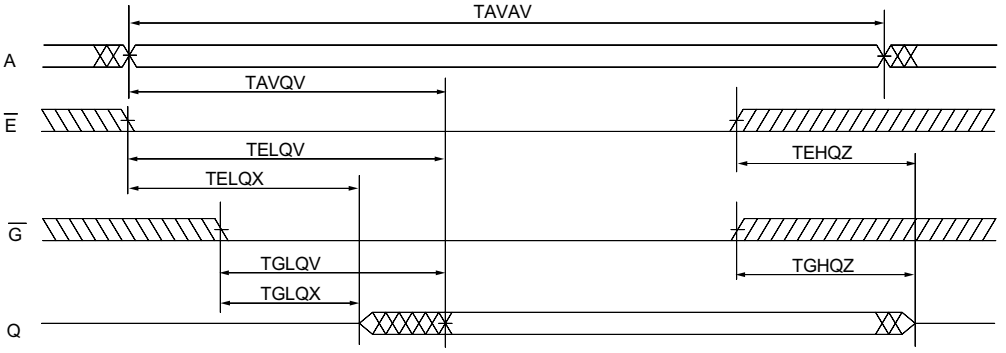
	Symbol		12ns		15ns		17ns		20ns		
Parameter	**JEDEC**	**Alt.**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Units**
Read Cycle Time	TAVAV	TRC	12		15		17		20		ns
Address Access Time	TAVQV	TAA		12		15		17		20	ns
Chip Enable Access Time	TELQV	TACS		10		10		15		20	ns
Chip Enable to Output in Low Z (1)	TELQX	TCLZ	3		3		3		3		ns
Chip Disable to Output in High Z (1)	TEHQZ	TCHZ		6		7		8		9	ns
Output Hold from Address Change	TAVQX	TOH	3		3		3		3		ns
Output Enable to Output Valid	TGLQV	TOE		6		7		8		9	ns
Output Enable to Output in Low Z (1)	TGLQX	TOLZ	3		3		3		3		ns
Output Disable to Output in High Z(1)	TGHQZ	TOHZ		6		7		8		9	ns

*Advanced Information

Read Cycle 1 - $\overline{W}$ High, $\overline{G}$, $\overline{E}$ Low



Read Cycle 2 - $\overline{W}$ High

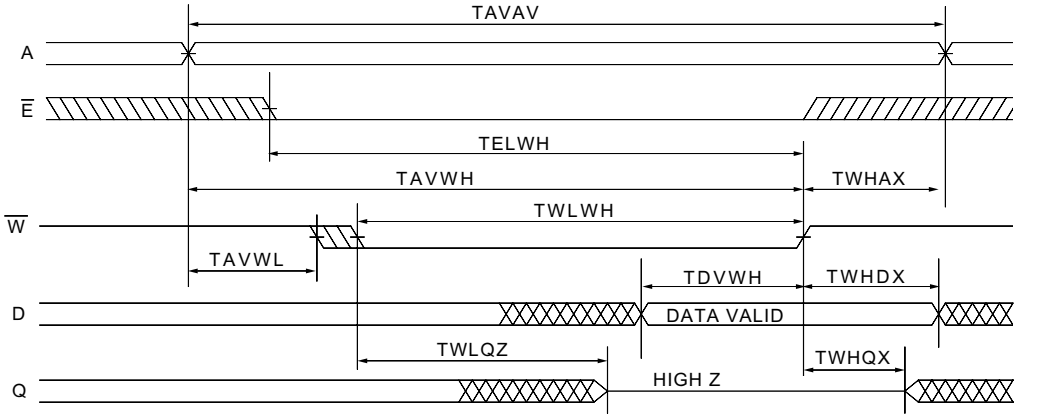


AC Characteristics Write Cycle

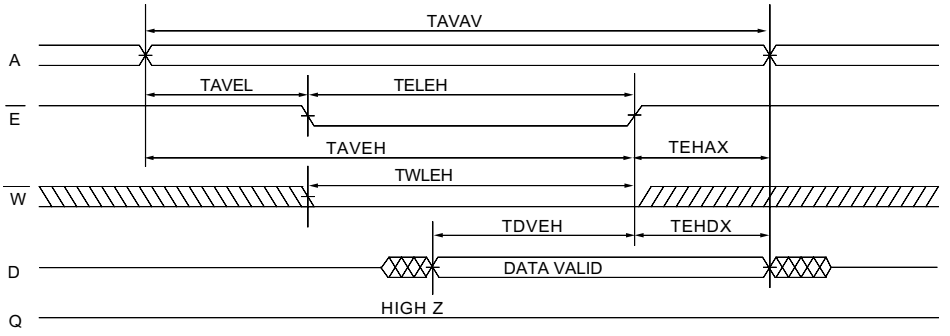
	Symbol		12ns		15ns		17ns		20ns		
Parameter	**JEDEC**	**Alt.**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Units**
Write Cycle Time	TAVAV	TWC	12		15		17		20		ns
Chip Enable to End of Write	TELWH	TCW	8		10		11		12		ns
	TELEH	TCW	8		10		11		12		ns
Address Setup Time	TAVWL	TAS	0		0		0		0		ns
	TAVEL	TAS	0		0		0		0		ns
Address Valid to End of Write	TAVWH	TAW	8		10		11		12		ns
	TAVEH	TAW	8		10		11		12		ns
Write Pulse Width	TWLWH	TWP	8		10		11		12		ns
	TWLEH	TWP	8		10		11		12		ns
Write Recovery Time	TWHAX	TWR	0		0		0		0		ns
	TEHAX	TWR	0		0		0		0		ns
Data Hold Time	TWHDX	TDH	0		0		0		0		ns
	TEHDX	TDH	0		0		0		0		ns
Write to Output in High Z (1)	TWLQZ	TWHZ	0	6	0	7	0	8	0	9	ns
Data to Write Time	TDVWH	TDW	6		7		8		9		ns
	TDVEH	TDW	6		7		8		9		ns
Output Active from End of Write (1)	TWHQX	TWLZ	3		3		3		3		ns

Note 1: Parameter guaranteed, but not tested.
*Advanced Information.

Write Cycle 1 - $\overline{W}$ Controlled



Write Cycle 2 - $\overline{E}$ Controlled



Ordering Information

Commercial (0°C to+70°C)

Part Number	Speed	Package
	(ns)	No.
EDI8L24512V12AC	12	99
EDI8L24512V15AC	15	99
EDI8L24512V17AC	17	99
EDI8L24512V20AC	20	99

Industrial (-40°C to+85°C)

Part Number	Speed	Package
	(ns)	No.
EDI8L24512V15AI	15	99
EDI8L24512V20AI	20	99

Package Description

Package No. 99
68 Lead PLCC
JEDEC MO-47AE