Digitally Controlled Programmable Gain Amplifier in SOT-23

FEATURES

- **3-Bit Digital Gain Control (0, 1, 2, 5, 10, 20, 50 and 100V/V)**
- **8-Pin TSOT-23 Package**
- **Rail-to-Rail Input Range**
- **Rail-to-Rail Output Swing**
- **Single or Dual Supply: 2.7V to 10.5V Total**
- 11MHz Gain Bandwidth Product
- 9nV/√Hz Input Noise at Gain of 100
- 120dB Total System Dynamic Range
- Input Offset Voltage: 3mV (Gain-of-1)
- Input Offset Voltage: 1.7mV (Gain-of-10)

APPLICATIONS

- Data Acquisition Systems
- Dynamic Gain Changing
- Automatic Ranging Circuits
- Automatic Gain Control

DESCRIPTION

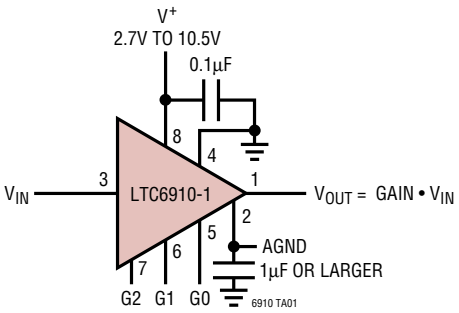
The LTC®6910-1 is a low noise digitally programmable gain amplifier (PGA) that is easy to use and occupies very little PC board space. The gain is adjustable using a 3-bit digital input to select gains of 0, 1, 2, 5, 10, 20, 50 and 100V/V.

The LTC6910-1 is an inverting amplifier with a rail-to-rail output. When operated with unity gain, the LTC6910-1 will also process rail-to-rail input signals. A half-supply reference generated internally at the AGND pin supports single power supply applications. Operating from single or split supplies from 2.7V to 10.5V, the LTC6910-1 is offered in an 8-lead TSOT-23 package. For versions with other gain ranges, see the LTC6910-2 and LTC6910-3 data sheets.

TYPICAL APPLICATION

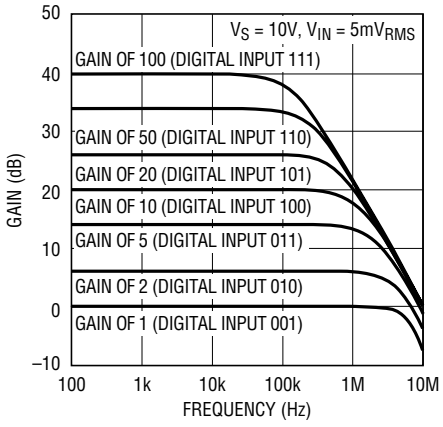
Single Supply Programmable Amplifier

GAIN	G2	G1	G0
0	0	0	0
–1	0	0	1
–2	0	1	0
–5	0	1	1
–10	1	0	0
–20	1	0	1
–50	1	1	0
–100	1	1	1



PIN 2 (AGND) PROVIDES BUILT-IN HALF-SUPPLY REFERENCE WITH INTERNAL RESISTANCE OF 5k. AGND CAN ALSO BE DRIVEN BY A SYSTEM ANALOG GROUND REFERENCE NEAR HALF SUPPLY

Frequency Response

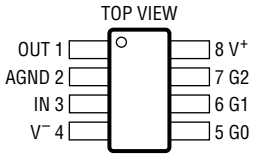


ABSOLUTE MAXIMUM RATINGS

(Note 1)

Total Supply Voltage (V+ to V–) 11V
Input Current ..... ±25mA
Operating Temperature Range (Note 2)
LTC6910-1C ..... –40°C to 85°C
LTC6910-1I ..... –40°C to 85°C
LTC6910-1H ..... –40°C to 125°C
Specified Temperature Range (Note 3)
LTC6910-1C ..... –40°C to 85°C
LTC6910-1I ..... –40°C to 85°C
LTC6910-1H ..... –40°C to 125°C
Storage Temperature Range ..... –65°C to 150°C
Lead Temperature (Soldering, 10 sec)..... 300°C

PACKAGE/ORDER INFORMATION



TS8 PACKAGE
8-LEAD PLASTIC TSOT-23

T_{JMAX} = 150°C, θ_{JA} = 230°C/W

ORDER PART NUMBER
LTC6910-1CTS8 LTC6910-1ITS8 LTC6910-1HTS8
TS8 PART MARKING*
LTB5

*The temperature grades are identified by a label on the shipping container. Consult LTC Marketing for parts specified with wider operating temperature ranges or other gain ranges.

GAIN SETTINGS AND PROPERTIES

Table 1

G2	G1	G0	NOMINAL VOLTAGE GAIN Volts/Volt	NOMINAL VOLTAGE GAIN (dB)	NOMINAL LINEAR INPUT RANGE (V_{P-P}) Dual 5V Supply	Single 5V Supply	Single 3V Supply	NOMINAL INPUT IMPEDANCE (kΩ)
0	0	0	0	–120	10	5	3	(Open)
0	0	1	–1	0	10	5	3	10
0	1	0	–2	6	5	2.5	1.5	5
0	1	1	–5	14	2	1	0.6	2
1	0	0	–10	20	1	0.5	0.3	1
1	0	1	–20	26	0.5	0.25	0.15	1
1	1	0	–50	34	0.2	0.1	0.06	1
1	1	1	–100	40	0.1	0.05	0.03	1

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications that apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_S = 5V, AGND = 2.5V, Gain = 1 (Digital Inputs 001), R_L = 10k to midsupply point, unless otherwise noted.

PARAMETER	CONDITIONS		LTC6910-1C LTC6910-1I MIN	TYP	MAX	LTC6910-1H MIN	TYP	MAX	UNITS
Voltage Gain (Note 4)	V_S = 2.7V, Gain = 1, R_L = 10k	●	–0.05	0	0.07	–0.06	0	0.07	dB
	V_S = 2.7V, Gain = 1, R_L = 500Ω	●	–0.1	–0.02	0.06	–0.12	–0.02	0.08	dB
	V_S = 2.7V, Gain = 2, R_L = 10k	●	5.96	6.02	6.08	5.96	6.02	6.08	dB
	V_S = 2.7V, Gain = 5, R_L = 10k	●	13.85	13.95	14.05	13.83	13.95	14.05	dB
	V_S = 2.7V, Gain = 10, R_L = 10k	●	19.7	19.9	20.1	19.7	19.9	20.1	dB
	V_S = 2.7V, Gain = 10, R_L = 500Ω	●	19.6	19.85	20.1	19.4	19.85	20.1	dB
	V_S = 2.7V, Gain = 20, R_L = 10k	●	25.7	25.9	26.1	25.65	25.9	26.1	dB
	V_S = 2.7V, Gain = 50, R_L = 10k	●	33.5	33.8	34.1	33.4	33.8	34.1	dB
	V_S = 2.7V, Gain = 100, R_L = 10k	●	39	39.6	40.2	38.7	39.6	40.2	dB
	V_S = 2.7V, Gain = 100, R_L = 500Ω	●	37.4	39	40.1	36.4	39	40.1	dB

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications that apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_S = 5V, AGND = 2.5V, Gain = 1 (Digital Inputs 001), R_L = 10k to midsupply point, unless otherwise noted.

PARAMETER	CONDITIONS		LTC6910-1C LTC6910-1I MIN	TYP	MAX	LTC6910-1H MIN	TYP	MAX	UNITS
Voltage Gain (Note 4)	V_S = 5V, Gain = 1, R_L = 10k	●	−0.05	0	0.07	−0.05	0	0.07	dB
	V_S = 5V, Gain = 1, R_L = 500Ω	●	−0.1	−0.01	0.08	−0.11	−0.01	0.08	dB
	V_S = 5V, Gain = 2, R_L = 10k	●	5.96	6.02	6.08	5.955	6.02	6.08	dB
	V_S = 5V, Gain = 5, R_L = 10k	●	13.8	13.95	14.1	13.75	13.95	14.1	dB
	V_S = 5V, Gain = 10, R_L = 10k	●	19.8	19.9	20.1	19.75	19.9	20.1	dB
	V_S = 5V, Gain = 10, R_L = 500Ω	●	19.6	19.85	20.1	19.45	19.85	20.1	dB
	V_S = 5V, Gain = 20, R_L = 10k	●	25.8	25.9	26.1	25.70	25.9	26.1	dB
	V_S = 5V, Gain = 50, R_L = 10k	●	33.5	33.8	34.1	33.4	33.8	34.1	dB
	V_S = 5V, Gain = 100, R_L = 10k	●	39.3	39.7	40.1	39.1	39.7	40.1	dB
	V_S = 5V, Gain = 100, R_L = 500Ω	●	38	39.2	40.1	37	39.2	40.1	dB
	V_S = ±5V, Gain = 1, R_L = 10k	●	−0.05	0	0.07	−0.05	0	0.07	dB
	V_S = ±5V, Gain = 1, R_L = 500Ω	●	−0.1	−0.01	0.08	−0.1	−0.01	0.08	dB
	V_S = ±5V, Gain = 2, R_L = 10k	●	5.96	6.02	6.08	5.96	6.02	6.08	dB
	V_S = ±5V, Gain = 5, R_L = 10k	●	13.80	13.95	14.1	13.80	13.95	14.1	dB
	V_S = ±5V, Gain = 10, R_L = 10k	●	19.8	19.9	20.1	19.75	19.9	20.1	dB
	V_S = ±5V, Gain = 10, R_L = 500Ω	●	19.7	19.9	20.1	19.6	19.9	20.1	dB
	V_S = ±5V, Gain = 20, R_L = 10k	●	25.8	25.95	26.1	25.75	25.95	26.1	dB
	V_S = ±5V, Gain = 50, R_L = 10k	●	33.7	33.85	34	33.6	33.85	34	dB
	V_S = ±5V, Gain = 100, R_L = 10k	●	39.4	39.8	40.2	39.25	39.8	40.2	dB
	V_S = ±5V, Gain = 100, R_L = 500Ω	●	38.8	39.6	40.1	38	39.6	40.1	dB
Signal Attenuation at Gain = 0 Setting	Gain = 0 (Digital Inputs 000), f = 20kHz	●		−122			−122		dB
Total Supply Voltage		●	2.7		10.5	2.7		10.5	V
Supply Current	V_S = 2.7V, V_{IN} = 1.35V	●		2	3		2	3	mA
	V_S = 5V, V_{IN} = 2.5V	●		2.4	3.5		2.4	3.5	mA
	V_S = ±5V, V_{IN} = 0V, Pins 5, 6, 7 = −5V or 5V	●		3	4.5		3	4.5	mA
	V_S = ±5V, V_{IN} = 0V, Pin 5 = 4.5V, Pins 6, 7 = 0.5V (Note 5)	●		3.5	4.9		3.5	4.9	mA
Output Voltage Swing LOW (Note 6)	V_S = 2.7V, R_L = 10k to Midsupply Point	●		12	30		12	30	mV
	V_S = 2.7V, R_L = 500Ω to Midsupply Point	●		50	100		50	100	mV
	V_S = 5V, R_L = 10k to Midsupply Point	●		20	40		20	40	mV
	V_S = 5V, R_L = 500Ω to Midsupply Point	●		90	160		90	160	mV
	V_S = ±5V, R_L = 10k to 0V	●		30	50		30	50	mV
	V_S = ±5V, R_L = 500Ω to 0V	●		180	250		180	250	mV
Output Voltage Swing HIGH (Note 6)	V_S = 2.7V, R_L = 10k to Midsupply Point	●		10	20		10	20	mV
	V_S = 2.7V, R_L = 500Ω to Midsupply Point	●		50	80		50	80	mV
	V_S = 5V, R_L = 10k to Midsupply Point	●		10	30		10	30	mV
	V_S = 5V, R_L = 500Ω to Midsupply Point	●		80	150		80	150	mV
	V_S = ±5V, R_L = 10k to 0V	●		20	40		20	40	mV
	V_S = ±5V, R_L = 500Ω to 0V	●		180	250		180	250	mV
Output Short-Circuit Current (Note 7)	V_S = 2.7V			±27			±27		mA
	V_S = ±5V			±35			±35		mA
AGND Open-Circuit Voltage	V_S = 5V	●	2.45	2.5	2.55	2.45	2.5	2.55	V

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications that apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_S = 5V, AGND = 2.5V, Gain = 1 (Digital Inputs 001), R_L = 10k to midsupply point, unless otherwise noted.

PARAMETER	CONDITIONS		LTC6910-1C LTC6910-1I MIN	TYP	MAX	LTC6910-1H MIN	TYP	MAX	UNITS
AGND (Common Mode) Input Voltage Range	V_S = 2.7V	●	0.55		1.6	0.7		1.5	V
	V_S = 5V	●	0.7		3.65	1.0		3.25	V
	V_S = ±5V	●	–4.3		3.5	–4.3		3.35	V
AGND Rejection (i.e., Common Mode Rejection or CMRR)	V_S = 2.7V, V_{AGND} = 1.1V to 1.6V	●	55	80		50	80		dB
	V_S = ±5V, V_{AGND} = –2.5V to 2.5V	●	55	75		50	75		dB
Power Supply Rejection Ratio (PSRR)	V_S = 2.7V to ±5V	●	60	80		60	80		dB
Offset Voltage Magnitude (Referred to Input)	Gain = 1	●		3.0	15		3.0	18	mV
	Gain = 10	●		1.7	10		1.7	12	mV
DC Input Resistance (Note 8)	DC V_{IN} = 0V								
	Gain = 0			>100			>100		MΩ
	Gain = 1	●		10			10		kΩ
	Gain = 2	●		5			5		kΩ
	Gain = 5	●		2			2		kΩ
	Gain = 10, 20, 50, 100	●		1			1		kΩ
DC Small-Signal Output Resistance	Gain = 0			0.4			0.4		Ω
	Gain = 1			0.7			0.7		Ω
	Gain = 2			1			1		Ω
	Gain = 5			1.9			1.9		Ω
	Gain = 10			3.4			3.4		Ω
	Gain = 20			6.4			6.4		Ω
	Gain = 50			15			15		Ω
	Gain = 100			30			30		Ω
Gain-Bandwidth Product	Gain = 100, f_{IN} = 200kHz		8	11	14	8	11	14	MHz
		●	6	11	16	5	11	16	MHz
Slew Rate	V_S = 5V, V_{OUT} = 2.8V_{P-P}			12			12		V/µs
	V_S = ±5V, V_{OUT} = 2.8V_{P-P}			16			16		V/µs
Wideband Noise (Referred to Input)	f = 1kHz to 200kHz								
	Gain = 0 Output Noise			3.8			3.8		μV_{RMS}
	Gain = 1			10.7			10.7		μV_{RMS}
	Gain = 2			7.3			7.3		μV_{RMS}
	Gain = 5			5.2			5.2		μV_{RMS}
	Gain = 10			4.5			4.5		μV_{RMS}
	Gain = 20			4.2			4.2		μV_{RMS}
	Gain = 50			3.9			3.9		μV_{RMS}
	Gain = 100			3.4			3.4		μV_{RMS}
Voltage Noise Density (Referred to Input)	f = 50kHz								
	Gain = 1			25			25		$nV/\sqrt{Hz}$
	Gain = 2			17			17		$nV/\sqrt{Hz}$
	Gain = 5			12			12		$nV/\sqrt{Hz}$
	Gain = 10			10			10		$nV/\sqrt{Hz}$
	Gain = 20			9.4			9.4		$nV/\sqrt{Hz}$
	Gain = 50			8.9			8.9		$nV/\sqrt{Hz}$
	Gain = 100			8.6			8.6		$nV/\sqrt{Hz}$
Total Harmonic Distortion	Gain = 10, f_{IN} = 10kHz, V_{OUT} = 1V_{RMS}			–90			–90		dB
				0.003			0.003		%
	Gain = 10, f_{IN} = 100kHz, V_{OUT} = 1V_{RMS}			–77			–77		dB
				0.014			0.014		%

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications that apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_S = 5V, AGND = 2.5V, Gain = 1 (Digital Inputs 001), R_L = 10k to midsupply point, unless otherwise noted.

PARAMETER	CONDITIONS		LTC6910-1C LTC6910-1I MIN	TYP	MAX	LTC6910-1H MIN	TYP	MAX	UNITS
Digital Input "High" Voltage	V_S = 2.7V	●	2.43			2.43			V
	V_S = 5V	●	4.5			4.5			V
	V_S = ±5V	●	4.5			4.5			V
Digital Input "Low" Voltage	V_S = 2.7V	●			0.27			0.27	V
	V_S = 5V	●			0.5			0.5	V
	V_S = ±5V	●			0.5			0.5	V

Note 1: Absolute Maximum Ratings are those values beyond which the life of the device may be impaired.

Note 2: The LTC6910-1C and LTC6910-1I are guaranteed functional over the operating temperature range of –40°C to 85°C. The LTC6910-1H is guaranteed functional over the operating temperature range of –40°C to 125°C.

Note 3: The LTC6910-1C is guaranteed to meet specified performance from 0°C to 70°C. The LTC6910-1C is designed, characterized and expected to meet specified performance from –40°C to 85°C but is not tested or QA sampled at these temperatures. LTC6910-1I is guaranteed to meet specified performance from –40°C to 85°C. The LTC6910-1H is guaranteed to meet specified performance from –40°C to 125°C.

Note 4: Gain is measured with a DC large-signal test using an output excursion between approximately 30% and 70% of supply voltage.

Note 5: Operating all three logic inputs at 0.5V causes the supply current to increase typically 0.1mA from this specification.

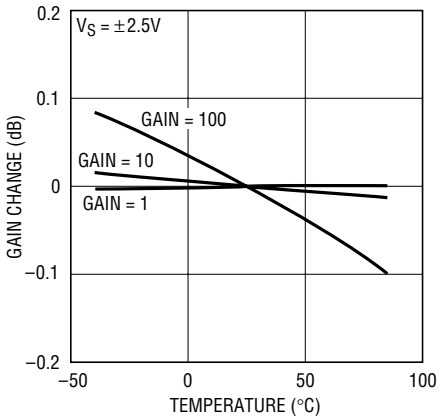
Note 6: Output voltage swings are measured as differences between the output and the respective supply rail.

Note 7: Extended operation with output shorted may cause junction temperature to exceed the 150°C limit and is not recommended.

Note 8: Input resistance can vary by approximately ±30% part-to-part at a given gain setting.

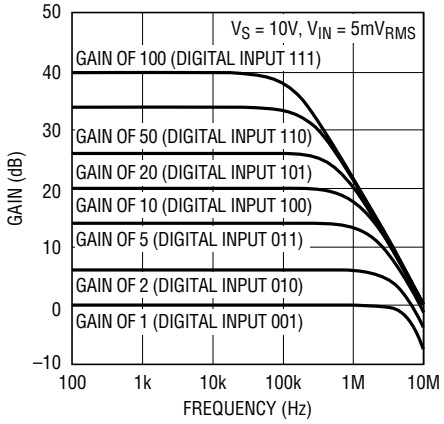
TYPICAL PERFORMANCE CHARACTERISTICS

Gain Shift vs Temperature



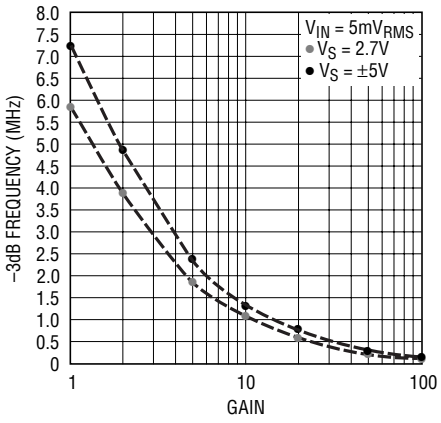
6910 G01

Frequency Response



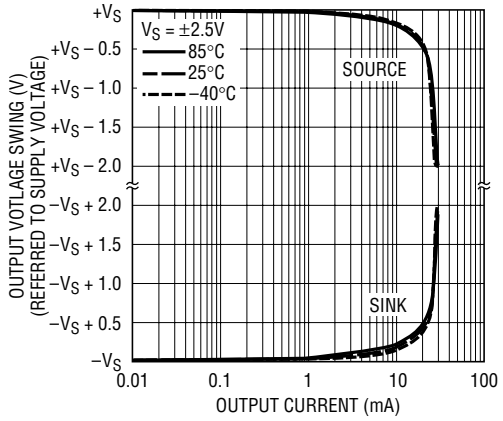
6910 G02

–3dB Bandwidth vs Gain Setting



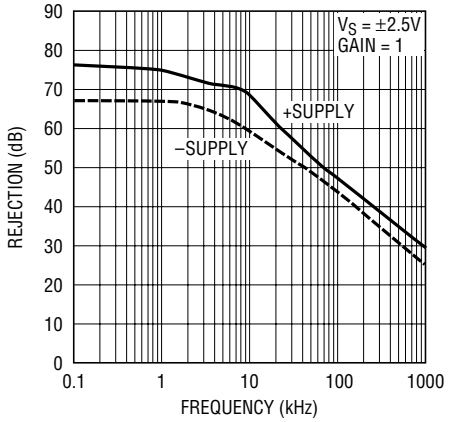
6910 G03

Output Voltage Swing vs Load Current



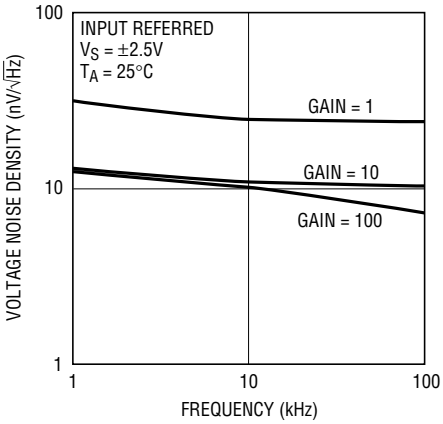
6910 G04

Power Supply Rejection vs Frequency



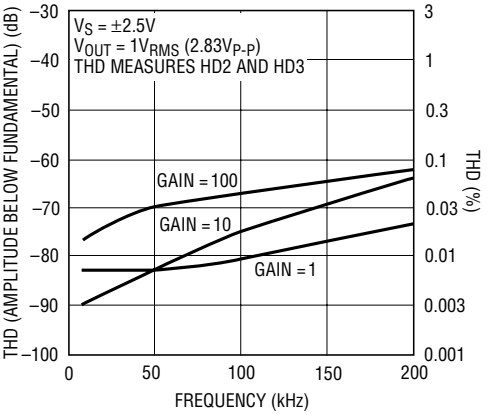
6910 G05

Noise Density vs Frequency



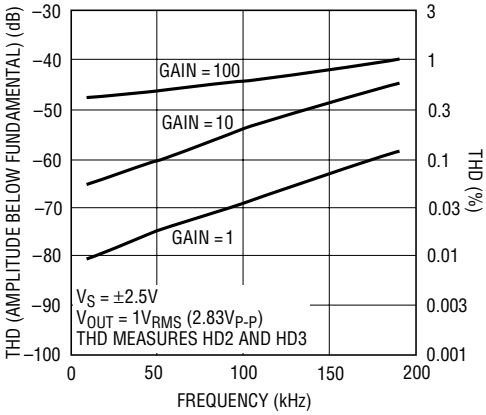
6910 G06

Distortion with Light Loading (R_L = 10k)



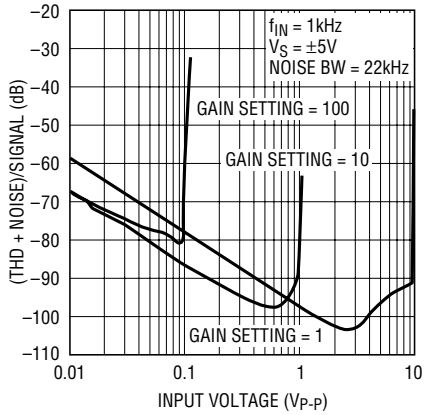
6910 G07

Distortion with Heavy Loading (R_L = 500Ω)



6910 G08

THD + Noise vs Input Voltage



6910 G09

PIN FUNCTIONS

OUT (Pin 1): Analog Output. This is the output of an internal operational amplifier and swings to near the power supply rails (V^+ and V^-) as specified in the Electrical Characteristics table. The internal op amp remains active at all times, including the zero gain setting (digital input 000). As with other amplifier circuits, loading the output as lightly as possible will minimize signal distortion and gain error. The Electrical Characteristics table shows performance at output currents up to 10mA and current limits that occur when the output is shorted to midsupply at 2.7V and ±5V supplies. Signal outputs above 10mA are possible but current-limiting circuitry will begin to affect amplifier performance at approximately 20mA. Long-term operation above 20mA output is not recommended. Do not exceed maximum junction temperature of 150°C. The output will drive capacitive loads up to 50pF. Capacitances higher than 50pF should be isolated by a series resistor to preserve AC stability.

AGND (Pin 2): Analog Ground. The AGND pin is at the midpoint of an internal resistive voltage divider, developing a potential halfway between the V^+ and V^- pins, with an equivalent series resistance to the pin of nominally 5kΩ (Figure 3). AGND is also the noninverting input of the internal op amp, which makes it the ground reference voltage for the IN and OUT pins. Because of this, very "clean" grounding is important, including an analog ground plane surrounding the package. For dual supply operation, this ground plane should be at zero volts and the AGND pin should connect directly to the ground plane (Figure 1). For single supply operation, in contrast, the V^- pin typically connects to system signal ground. The ground plane should then tie to V^- and the AGND pin should be AC-bypassed to the ground plane (Figure 2) by at least a 1µF high quality capacitor.

In noise-sensitive single-supply applications, it is important to AC-bypass the AGND pin. Otherwise wideband noise will enter the signal path from the internal voltage-divider resistors that set the DC voltage on AGND in single-supply applications. This noise can reduce SNR by 3dB at high gain settings. The resistors present a Thévenin equivalent of approximately 5k to the AGND pin. An external capacitor from AGND to the ground plane, whose impedance is well below 5k at frequencies of interest, will suppress this noise. A 1µF high quality capacitor is effective for frequencies down to 1kHz. Larger capacitors extend this suppression to proportionately lower frequencies. This issue does not arise in dual supply applications because AGND goes directly to ground.

In applications requiring an analog ground reference other than half the total supply voltage, the user can override the built-in analog ground reference by tying the AGND pin to a reference voltage within the AGND voltage range specified in the Electrical Characteristics table. The AGND pin will load the external reference with approximately 5k

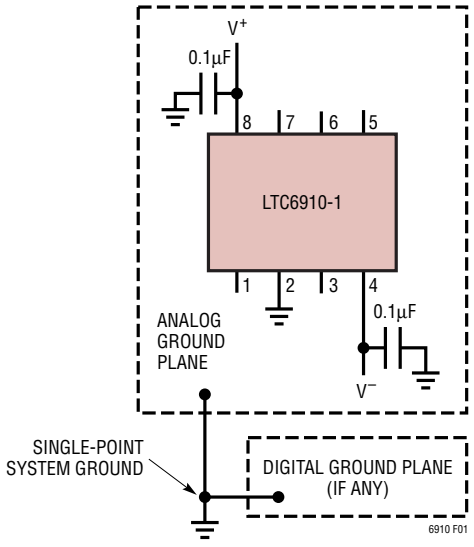


Figure 1. Dual Supply Ground Plane Connection

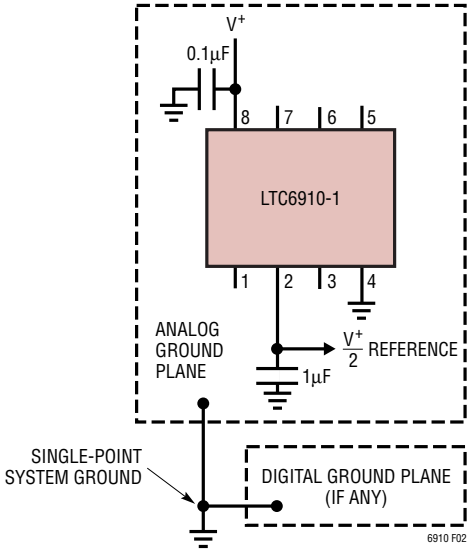


Figure 2. Single Supply Ground Plane Connection

PIN FUNCTIONS

returned to the half-supply potential. AGND should still be capacitively bypassed to a ground plane as noted above. Do not connect the AGND pin to the V^- pin.

IN (Pin 3): Analog Input. The input signal to the amplifier in the LTC6910-1 is the voltage difference between the IN and AGND pins. The IN pin connects internally to a digitally controlled resistance whose other end is a current summing point at the same potential as the AGND pin (Figure 3). At unity gain (digital input 001), the value of this input resistance is approximately 10kΩ and the IN voltage range is rail-to-rail (V^+ to V^-). At gain settings above unity (digital input 010 or higher), the input resistance falls, to nominally 1kΩ at gain settings of 10V/V or greater (digital input 100 or greater). Also, the linear input range falls in inverse proportion to gain. (The higher gains are designed to boost lower level signals with good noise performance.) In the "zero" gain state (digital input 000), analog switches disconnect the IN pin internally and this pin presents a very high input resistance. The input may vary from rail to rail in the "zero" gain setting but the output is insensitive to it and remains at the AGND potential. Table 1 summarizes the LTC6910's behavior for all gain codes. Circuitry driving the IN pin must consider the LTC6910-1's input resistance and the variation of this resistance when used at multiple gain settings. Signal sources with significant output resistance may introduce a gain error as the source's output resistance and the LTC6910-1's input resistance form a voltage divider. This is especially true at the higher gain settings where the input resistance is lowest.

In single supply voltage applications at elevated gain settings (digital input 010 or higher), it is important to remember that the LTC6910-1's DC ground reference for both input and output is AGND, not V^-. With increasing gains, the LTC6910-1's input voltage range for unclipped output is no longer rail-to-rail but shrinks toward AGND. The OUT pin also swings positive or negative with respect to AGND. At unity gain (digital input 001), both IN and OUT voltages can swing from rail to rail (Table 1).

V^-, V^+ (Pins 4, 8): Power Supply Pins. The V^+ and V^- pins should be bypassed with 0.1µF capacitors to an adequate analog ground plane using the shortest possible wiring. Electrically clean supplies and a low impedance ground are important for the high dynamic range available from the LTC6910-1 (see further details under AGND). Low noise linear power supplies are recommended. Switching power supplies require special care to prevent switching noise coupling into the signal path, reducing dynamic range.

G0, G1, G2 (Pins 5, 6, 7): CMOS-Level Digital Gain-Control Inputs. G2 is the most significant bit (MSB). These pins control the voltage gain from IN to OUT pins. In the LTC6910-1, the voltage gain range is 0 to 100V/V in eight discrete values 0, 1, 2, 5, 10, 20, 50, 100, set respectively by digital inputs 000 through 111 (or in decimal form, 0 through 7). Digital input code 000 causes a "zero" gain with very low output noise. In this "zero" gain state the IN pin is disconnected internally, but the OUT pin remains active and forced by the internal op amp to the voltage present on the AGND pin. Note that the voltage gain is inverting: OUT and IN pins always swing on opposite sides of the AGND potential. The G pins are high impedance CMOS logic inputs and must be connected (they will float to unpredictable voltages if open circuited). Table 1 summarizes the effects of the G-pin code. No speed limitation is associated with the digital logic because it is memoryless and much faster than the analog signal path.

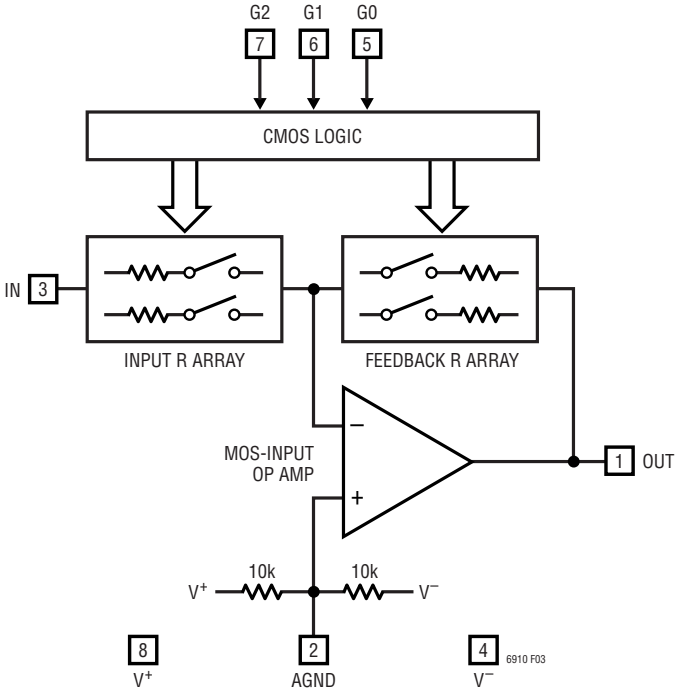


Figure 3. Block Diagram

APPLICATIONS INFORMATION

Functional Description

The LTC6910-1 is a small outline, wideband inverting DC amplifier whose voltage gain is digitally programmable. It delivers a choice of eight voltage gains, controlled by the 3-bit digital inputs to the G pins, which accept CMOS logic levels. The gain code is always monotonic; an increase in the 3-bit binary number (G2 G1 G0) causes an increase in the gain. LTC6910-1's nominal gain magnitudes are 0, 1, 2, 5, 10, 20, 50, and 100Volts/Volt (like a gain knob on an instrument). Gain control within the amplifier occurs by switching resistors from a matched array in or out of a closed-loop op amp circuit using MOS analog switches (Figure 3). Bandwidth depends on gain setting. The lower gains of 1, 2 and 5V/V (digital inputs 001-011) exhibit respective –3dB frequencies of 7, 5 and 2.5MHz at a ±5V supply. Gain settings from 10 to 100 (digital inputs 100-111) give constant gain bandwidth intercept of approximately 11MHz.

Digital Control

Logic levels for the LTC6910-1 digital gain control inputs (Pins 5, 6, 7) are nominally rail-to-rail CMOS. Logic 1 is V^+, logic 0 is V^- or alternatively 0V when using ±5V supplies. The part is tested with the values listed in the Electrical Characteristics table (Digital Input "High" and "Low" Voltages), which are 10% and 90% of full excursion on the inputs. That is, the tested logic levels are 0.27V and 2.43V with a 2.7V supply, 0.5V and 4.5V levels with 0V and 5V supply rails, and 0.5V and 4.5V logic levels at ±5V supplies. Do not attempt to drive the digital inputs with TTL logic levels. TTL sources should be adapted with suitable pull-up resistors to 5V so that they will swing to the positive rail.

AC-Coupled Operation

Adding a capacitor in series with the IN pin makes the LTC6910-1 into an AC-coupled amplifier, suppressing the source's DC level (also reducing the offset voltage from the LTC6910-1 itself). No further components are required because the input of the LTC6910-1 biases itself correctly when a series capacitor is added. The IN pin connects to an internal variable resistor (and floats when DC open-circuited to a well defined voltage equal to the AGND input voltage at nonzero gain settings). The value of this internal input resistor varies between 10k and 1k at LTC6910-1 gain settings of 1V/V to 100V/V (the rightmost column in Table 1). Therefore, with a series input capacitor the low frequency cutoff will also vary with gain. For example, for a low frequency corner of 1kHz or lower, use a series capacitor of 0.16µF or larger. 0.16µF has a reactance of 1kΩ at 1kHz, giving a 1kHz lower –3dB frequency for gain settings of 10V/V through 100V/V. If the LTC6910-1 is operated at lower gain settings with an 0.16µF input capacitor, the higher input resistance will reduce the lower corner frequency down to 100Hz at a gain setting of 1V/V. These frequencies scale inversely with the value of the input capacitor.

Note that operating the LTC6910-1 in zero gain mode (digital inputs 000) open circuits the IN pin and this demands some care if employed with a series input capacitor. When the chip enters the zero gain mode, the opened IN pin tends to freeze the voltage across the capacitor to the value it held just before the zero gain state. This can place the IN pin at or near the DC potential of a supply rail (the IN pin may also drift to a supply potential in this state due to small junction leakage currents). To prevent driving the IN pin outside the supply limit and potentially damaging the chip, avoid AC input signals in the zero gain state with a series capacitor. Also, switching later to a nonzero gain value will cause a transient pulse at the output of the LTC6910-1 (with a time constant set by the capacitor value and the new LTC6910-1 input resistance value). This occurs because the IN pin returns to the AGND potential and transient current flows to charge the capacitor to a new DC drop.

Construction and Instrumentation Cautions

Electrically clean construction is important in applications seeking the full dynamic range of the LTC6910-1 amplifier. Short, direct wiring will minimize parasitic capacitance and inductance. High quality supply bypass capacitors of 0.1µF near the chip provide good decoupling from a clean, low inductance power source. But several cm of wire (i.e., a few microhenrys of inductance) from the power supplies, unless decoupled by substantial capacitance (≥10µF) near the chip, can cause a high-Q LC resonance

TYPICAL APPLICATIONS

in the hundreds of kHz in the chip's supplies or ground reference. This may impair circuit performance at those frequencies. A compact, carefully laid out printed circuit board with a good ground plane makes a significant difference in minimizing distortion. Finally, equipment to measure amplifier performance can itself introduce distortion or noise floors. Checking for these limits with a wire replacing the chip is a prudent routine procedure.

Expanding an ADC's Dynamic Range

Figure 4 shows a compact data acquisition system for wide ranging input levels. This figure combines an LTC6910-1 programmable amplifier (8-lead TSOT-23) with an LTC1864 analog-to-digital converter (ADC) in an 8-lead MSOP. This ADC has 16-bit resolution and a maximum sampling rate of 250ksps. The LTC6910-1 expands the ADC's input amplitude range by 40dB while operating from the same single 5V supply. The 499Ω resistor and 270pF capacitor couple cleanly between the LTC6910-1's output and the switched-capacitor input of the LTC1864.

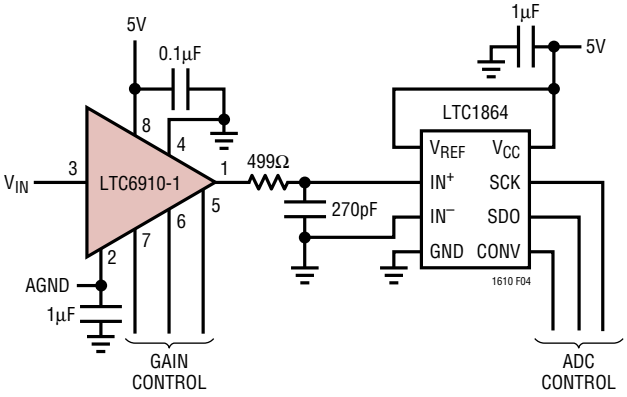


Figure 4. Expanding an ADC's Dynamic Range

At a gain setting of 10V/V in the LTC6910-1 (digital input 100) and a 250ksps sampling rate in the LTC1864, a 10kHz input signal at 60% of full scale shows a THD of –87dB at the digital output of the ADC. 100kHz input signals under the same conditions produce THD values around –75dB. Noise effects (both random and quantization) in the ADC are divided by the gain of the amplifier when referred to V_{IN} in Figure 4. Because of this, the circuit can acquire a signal that is 40dB down from full scale of $5V_{P-P}$ with an SNR of over 70dB. Such performance from an ADC alone (70 + 40 = 110dB of useful dynamic range at 250ksps), if available, would be far more expensive.

Low Noise AC Amplifier with Programmable Gain and Bandwidth

Analog data acquisition can exploit band limiting as well as gain to suppress unwanted signals or noise. Tailoring an analog front end to both the level and bandwidth of each source maximizes the resulting SNR.

Figure 5 shows a block diagram and Figure 6 the practical circuit for a low noise amplifier with gain and bandwidth independently programmable over 100:1 ranges. One LTC6910-1 controls the gain and another controls the

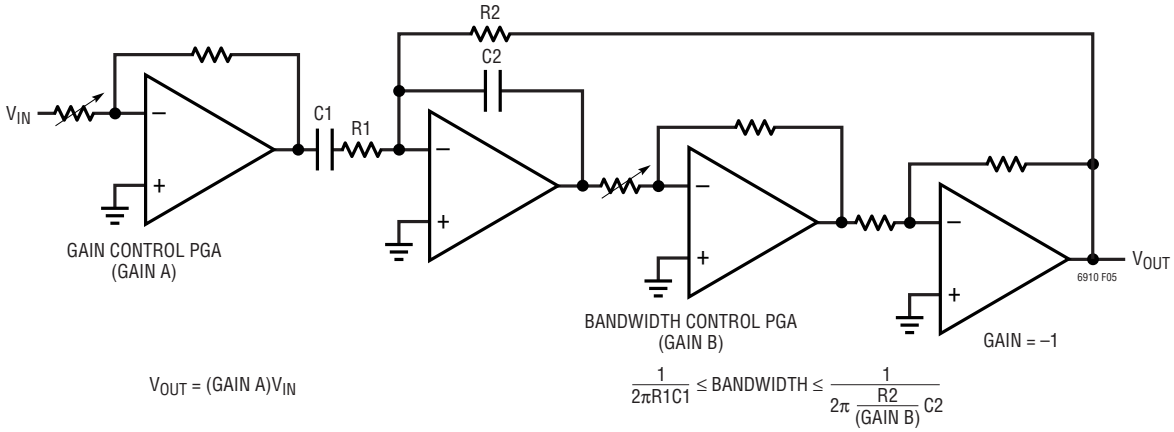
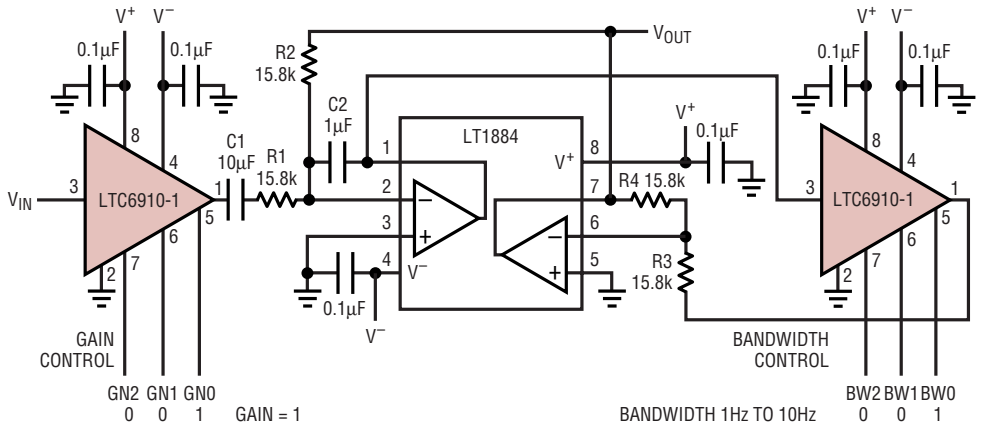


Figure 5. Block Diagram of an AC Amplifier with Programmable Gain and Bandwidth

TYPICAL APPLICATIONS

bandwidth. An LT1884 dual op amp forms an integrating lowpass loop with capacitor C2 to set the programmable upper corner frequency. The LT1884 also supports rail-to-rail output swings over the total supply voltage range of 2.7V to 10.5V. AC coupling through capacitor C1 establishes a fixed low frequency corner of 1Hz, which can be adjusted by changing C1. Alternatively, shorting C1 makes the amplifier DC coupled. (If DC gain is not needed, however, the AC coupling suppresses several error sources: any shifts in DC levels, low frequency noise and all amplifier DC offset voltages other than the low internally trimmed LT1884 offset in the integrating amplifier.)

Measured frequency responses in Figure 6 demonstrate bandwidth settings of 10Hz, 100Hz and 1kHz, with digital codes at the BW inputs of respectively 001, 100 and 111, and unity gain in each case. By scaling C2, this circuit can serve other frequency ranges, such as a maximum of 10kHz with 0.1µF using LT1884 (gain-bandwidth product around 1MHz). Noise floor from internal sources yields an output SNR of 76dB with $10mV_{P-P}$ input, gain of 100 and 100Hz bandwidth; for $100mV_{P-P}$ input, gain of 10 and 1000Hz bandwidth it is 64dB.



GN2	GN1	GN0	
0	0	1	GAIN = 1
0	1	0	GAIN = 2
0	1	1	GAIN = 5
1	0	0	GAIN = 10
1	0	1	GAIN = 20
1	1	0	GAIN = 50
1	1	1	GAIN = 100

	BW2	BW1	BW0
BANDWIDTH 1Hz TO 10Hz	0	0	1
BANDWIDTH 1Hz TO 20Hz	0	1	0
BANDWIDTH 1Hz TO 50Hz	0	1	1
BANDWIDTH 1Hz TO 100Hz	1	0	0
BANDWIDTH 1Hz TO 200Hz	1	0	1
BANDWIDTH 1Hz TO 500Hz	1	1	0
BANDWIDTH 1Hz TO 1000Hz	1	1	1

Gain vs Frequency

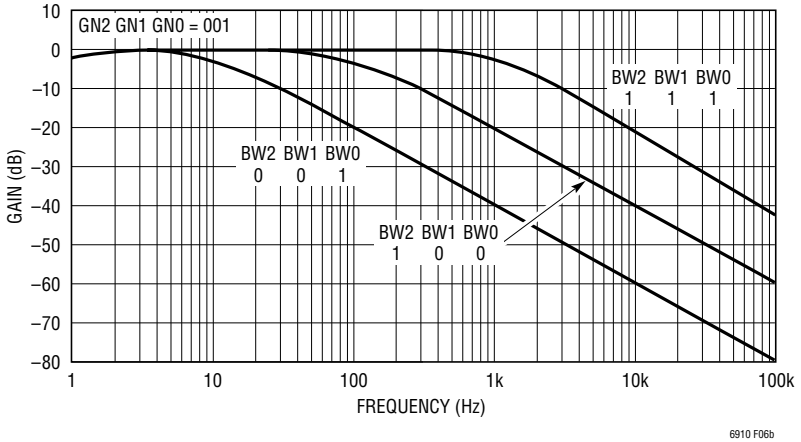


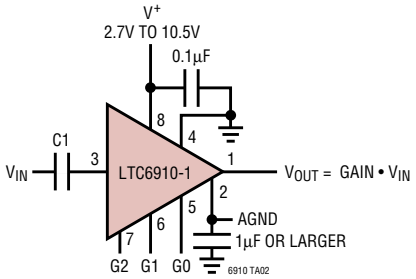
Figure 6. Low Noise AC Amplifier with Programmable Gain and Bandwidth

TYPICAL APPLICATION

AC-Coupled Amplifiers

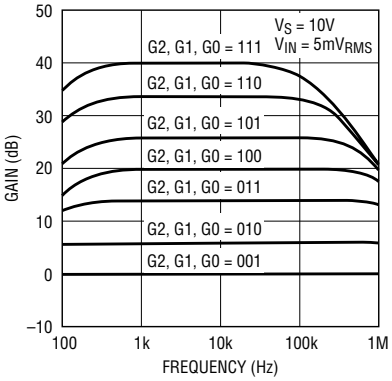
PASSBAND GAIN	G2	G1	G0	LOWER –3dB FREQ WITH C1 = 1µF
0	0	0	0	—
–1	0	0	1	16Hz
–2	0	1	0	32Hz
–5	0	1	1	80Hz
–10	1	0	0	160Hz
–20	1	0	1	160Hz
–50	1	1	0	160Hz
–100	1	1	1	160Hz

C1 VALUE SETS LOWER CORNER FREQUENCY. THE TABLE SHOWS THIS FREQUENCY WITH C1 = 1µF. THIS FREQUENCY SCALES INVERSELY WITH C1



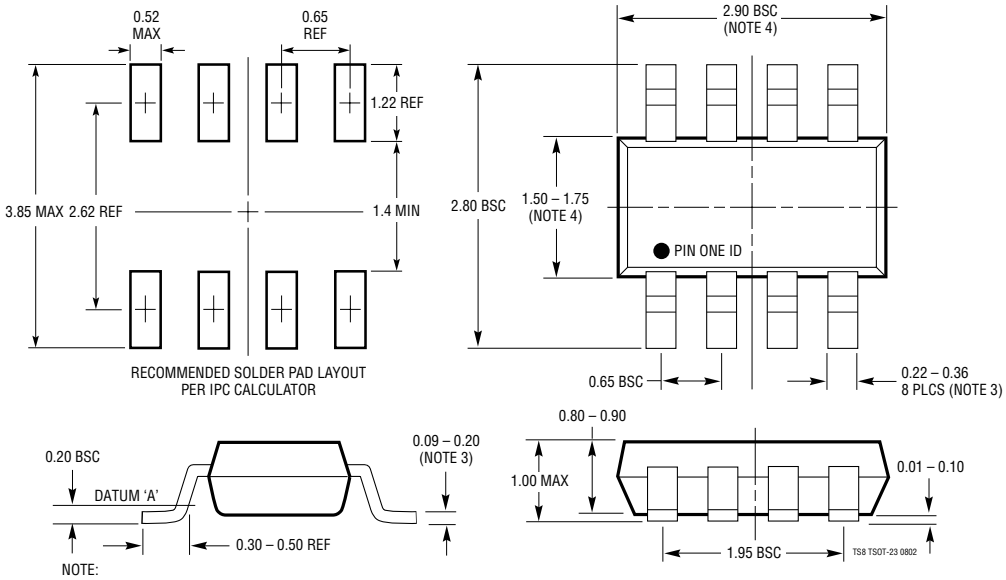
PIN 2 (AGND) SETS DC OUTPUT VOLTAGE AND HAS BUILT-IN HALF-SUPPLY REFERENCE WITH INTERNAL RESISTANCE OF 5k. AGND CAN ALSO BE DRIVEN BY A SYSTEM ANALOG GROUND REFERENCE NEAR HALF SUPPLY

Frequency Response



PACKAGE DESCRIPTION

TS8 Package
8-Lead Plastic TSOT-23
(Reference LTC DWG # 05-08-1637)



NOTE:
1. DIMENSIONS ARE IN MILLIMETERS
2. DRAWING NOT TO SCALE
3. DIMENSIONS ARE INCLUSIVE OF PLATING
4. DIMENSIONS ARE EXCLUSIVE OF MOLD FLASH AND METAL BURR
5. MOLD FLASH SHALL NOT EXCEED 0.254mm
6. JEDEC PACKAGE REFERENCE IS MO-193

RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LT®1228	100MHz Gain Controlled Transconductance Amplifier	Differential Input, Continuous Analog Gain Control
LT1251/LT1256	40MHz Video Fader and Gain Controlled Amplifier	Two Input, One Output, Continuous Analog Gain Control
LTC1564	10kHz to 150kHz Digitally Controlled Filter and PGA	Continuous Time, Low Noise 8th Order Filter and 4-Bit PGA
LTC6910-2	Digitally Controlled PGA	SOT-23, Gains 0, 1, 2, 4, 8, 16, 32, 64V/V
LTC6910-3	Digitally Controlled PGA	SOT-23, Gains 0, 1, 2, 3, 4, 5, 6, 7V/V

Linear Technology Corporation
1630 McCarthy Blvd., Milpitas, CA 95035-7417
(408) 432-1900 • FAX: (408) 434-0507 • www.linear.com
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