PACSZ1284 Single Chip IEEE 1284 Termination Network

Introduction

Personal computers, notebooks, servers, workstations and peripherals, like printers, can be connected through a parallel port. Both sides of this interconnection must implement a parallel port interface that is compliant with the IEEE 1284 standard. That is achieved by using termination, pull-up resistors and EMI filtering on the bus lines. In addition, government EMC regulations limit the EMI/RFI emissions and therefore impose filtering on the parallel port. Also, motherboards and peripherals must be immune to electrostatic discharge (ESD). California Micro Devices is addressing all these requirements and offers an integrated solution aimed to simplify the design and manufacturing phases.

IEEE 1284 single chip solutions

California Micro Devices provides complete solution for IEEE 1284 termination, filtering, pull-up, and ESD protection, in a single QSOP 28-pin package. The IEEE 1284 single chip solutions consist of the PACS1284, PACSE1284, and PACSZ1284. These parts are up-graded versions of CAMD original 2 chip solutions with the PAC1284 or the PRC1284. The PACSZ1284 is the latest addition to the family, featuring improved ESD protection, a remarkable four fold to eight fold improvement in ESD protection over previous offerings.

The PACSx1284 devices terminate all 17 lines of the IEEE 1284 parallel port. It complies to the IEEE 1284 standard by integrating pull-up resistors on all 17 lines, series resistors on 9 lines, and filtering capacitors on all lines. Table 1 summarized all these parameters.

The table column labeled “ESD” specifies the contact discharge ESD protection per the IEC61000-4-2 standard for all pins to be connected to the parallel port connector, these are pin numbers 1, 2, 8, 10, 12, 15, 16, 17, 18, 19, 21, 23 to 28.

Figure 1 illustrates the PACSx1284 circuit schematic. ESD protection elements are represented on the figure with diodes in parallel to the filter capacitors.

IEEE1284 SINGLE CHIP SOLUTIONS					
Part Number	**ESD (KV)**	**R1 (Ω) Pull-up**	**R2 (Ω) Series**	**C (pF)**	**RC Code**
PACS1284-02	4	2.2K	33	220	02
PACS1284-04	4	4.7K	33	180	04
PACS1284-05	4	4.7K	33	100	05
PACSE1284-02	8	2.2K	33	220	02
PACSE1284-04	8	4.7K	33	180	04
PACSZ1284-01	30	1K	33	150	01
PACSZ1284-02	30	2.2K	33	150	02

Table 1

PACSZ1284 CIRCUIT SCHEMATIC

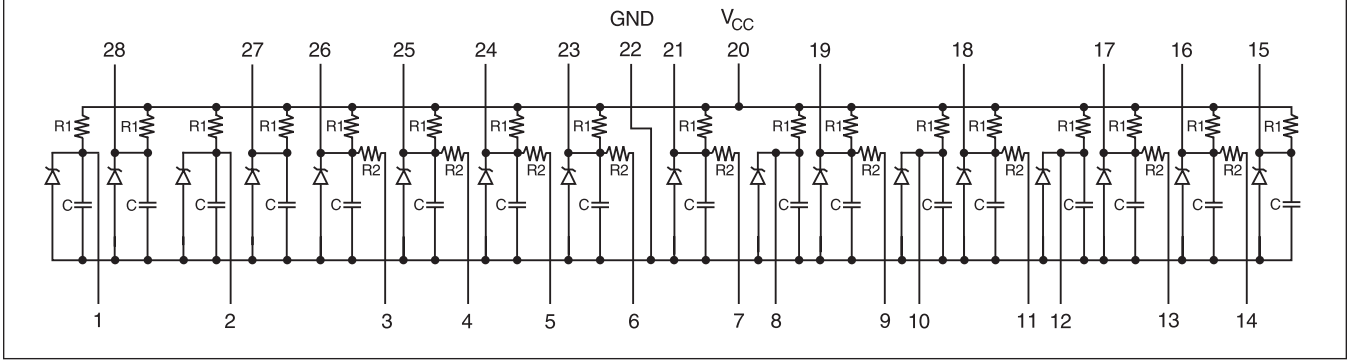

Figure 1

IEEE 1284 Specification

The ECP (Extended Capabilities Port) Mode is one of the communication modes which is asynchronous, byte-wide, and bidirectional. It communicates with the peripheral in an interlocked handshake. The EPP (Enhanced Parallel Port) Mode is an asynchronous, byte-wide, and bidirectional channel controlled by the host device. The enhanced interface is able to exchange data at 2 Mega bytes per second. Peripherals such as printers, removable backup drives, set-top-boxes, scanners, external LAN adapters or home-phone line adapters can be connected to the parallel port.

Figure 2 shows the placement of the PACSZ1284 Termination Network between the parallel port I/O controller and the connector.

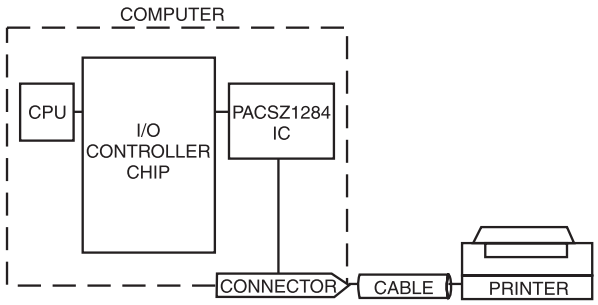

Figure 2

The IEEE 1284 specifications for bi-directional parallel peripheral interface for PCs defines two levels of interface compatibility, Level I and Level II. The Level I interface is defined for products that are not going to operate at the high speed advanced modes, but need to take advantage of the reverse channel capabilities of the standard. The Level II interface is for devices that will operate in the advanced modes, with long cables, and at the higher data rates. The PACSZ1284 complies with the IEEE 1284 specifications for both Level I and Level II types of interfaces [refer to Section 8.3, Electrical Characteristics of IEEE 1284 Specifications].

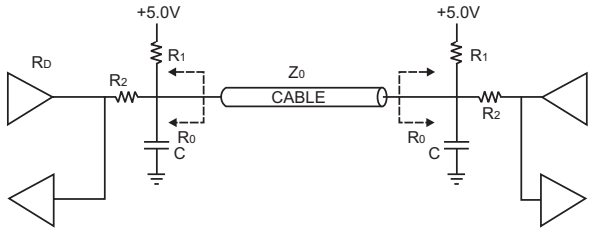

Figure 3

Figure 3 shows the recommended termination for the Level II transceiver interface. R0 represents the output impedance at the connector. R2 and R1 are the series and the pull-up resistors respectively. C is the shunt filter capacitor. Z0 is the characteristic impedance of the cable connecting the peripheral with the PC. R_D is the output impedance of the transceiver. The table of standard values from Table 1 gives a popular set of component values for R1, R2, and C to choose from, depending upon the kind of application.

The following sections of this application note discuss series termination, function of the pull-up resistor, EMC regulations, low pass RC filter, and ESD protection.

Series Termination

Unlike parallel, Thevenin or AC termination techniques, series termination focuses on the transmitting end of the cable. The series termination resistor (R2 from the schematic) is placed between the driver and the connector. The termination resistor and the characteristic impedance of the line combine to form a voltage divider that attenuates the transmitted signal to half its value. At the receiving end, however, the mismatch between the line impedance and the input impedance (typically, very high) of the receiver will cause a reflection of approximately the same voltage magnitude as the incident signal. The receiving device will immediately see the full voltage (sum of incident and reflected voltages) and the added signal propagates to the driver end. There will be no further reflections as the reflected wave gets terminated at the driver end by the series termination device.

Series termination is widely used with advanced CMOS devices, because this technique adds no extra impedance from the line to ground path of the signal. When used with devices from the FACT logic family, the series termination increases the impedance present at the output of the drivers; therefore, the drivers dissipate less power than they would without the termination. Unlike some parallel termination techniques, series termination adds no DC load to the drivers. Series termination is preferred when the load is lumped at the end of the cable or when a minimum number of components is required. The only constraint in determining the value of the series termination resistor is that it should match the value of the characteristic impedance of the line minus the output impedance of the driver as close as possible. Table 1 lists the values of the series termination resistor R2 available with the PACSZ1284.

Pull-Up Resistor

The resistor R1 is a pull-up resistor because it serves to pull the voltage on the line to a high. Most transients on the supply voltage are too short to charge the capacitor connected to the ground through the pull-up resistor. Therefore, the receiver is protected against temporary overvoltages. The value of the pull-up resistor depends on the family of the logic device used as the driver. For

example, TTL devices having an *open-collector* output will not function properly until a pull-up resistor (a few kilo ohms) is connected. Table 1 lists the values of the pull-up resistor R1.

EMC Regulations

Electromagnetic Compatibility (EMC) is the ability of an electronic system to (1) function properly in its intended electromagnetic environment (*i.e.,* immunity), and (2) not be a source of pollution to that environment (*i.e.,* emission). EMC design can be approached in either of two ways: one is the *crisis approach,* and the other is the *systems approach*. In the crisis approach the designer proceeds with a total disregard of EMC until the design is finished, and testing or—worse yet—field experience suggests that a problem exists. Solutions, implemented at this late stage, are usually expensive and consist of undesirable "add-ons". This is often referred to as the "band-aid" approach. On the other hand, the systems approach considers EMC throughout the design.

As system development progresses from design to testing and to production, the variety of noise mitigation techniques available to the designer decreases steadily. Concurrently, cost goes up. These trends are shown in Figure 4. Early solutions to interference problems, therefore, are usually best and least expensive.

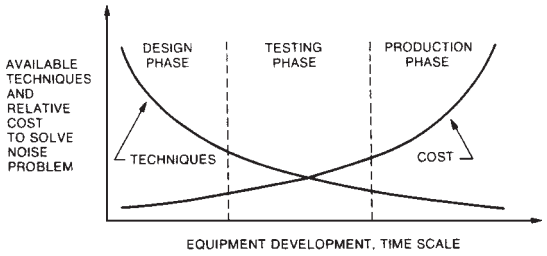

Figure 4

In the United States, the Federal Communications Commission (FCC) regulates the use of radio and wire communications. Part of its responsibility concerns the control of interference. According to FCC regulations (Parts 15 & 18), emissions must not exceed certain maximum levels depending on whether the equipment is for strictly industrial use (Class A equipment) or also for residential use (Class B equipment). Figure 5 shows graphically these limitations for Class A and Class B equipment. As can be seen, the Class B limits are more restrictive by about a factor of 3 (10 dB).

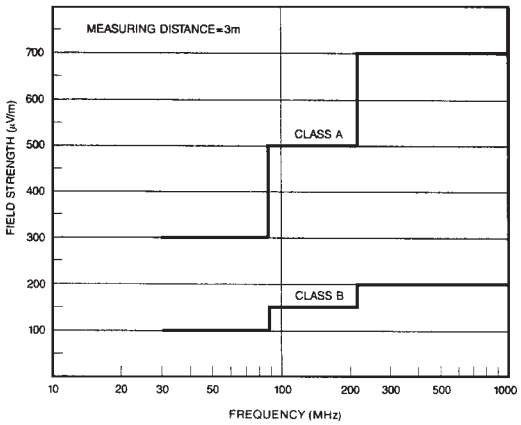

Figure 5

Several approaches are available today to control EMI/RFI emissions, including grounded metal enclosures, judicious component placement and interconnect designs, power-supply decoupling, and low-pass filtering of signal lines.

CAMD's PACSZ1284 has a RC low pass filter network integrated with the termination components to mitigate EMI/RFI radiation.

Low Pass RC Filter

Low pass filtering is effective for EMI/RFI filtering when the noise components to be rejected occur at frequencies higher than the signal frequency to be passed. The sources of noise could either be intrinsic or extrinsic. Intrinsic noise includes random fluctuations within physical systems, higher harmonic components of the digital signal, etc. Extrinsic noise source, includes voltage coupling through common ground impedance (crosstalk voltage), noises from the power source, and noise due to natural disturbances, such as lightning and sunspots.

In a one pole RC filter circuit, the capacitor forms an AC ground for the high frequency noise and hence filters noise to the ground. The signal frequency components suffer insertion loss (very small) due to the series impedance on the line and are much less attenuated by the shunt impedance between the line and ground as compared to the high frequency components (noise).

Figure 6 shows the typical insertion loss of the PACSZ1284 vs. frequency.

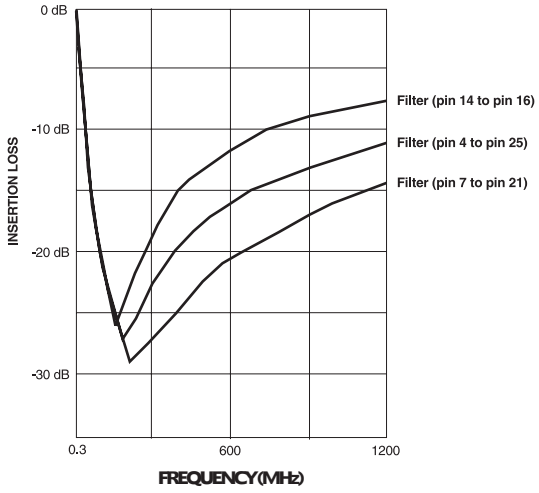

Figure 6. PACSZ1284 Insertion Loss (Typical)

The factors determining the choice of R and C values for PACSZ1284 are as follows.

The RC combination (also referred to as *time constant*) of the filter adds to the existing system RC delay. This addition must not exceed the sampling window of the receiving IC. The signal attenuation due to the series impedance on the line can be minimized by choosing small R values relative to the load impedance. The available values for R and C from Table 1 provides sufficient attenuation at high frequency, thus controlling the overall emission.

ESD Protection

Energy from a static discharge can be coupled to an electronic circuit either by direct conduction of discharge current or through capacitive/inductive couplings. ESD-induced effects in electronic circuits could be a tolerable transient upset, a false triggering of logic circuits, or even damage of the hardware itself. A circuit or system may be protected from a static discharge by providing an alternate path for the discharge current to bypass the circuit. In the PACSZ1284, ESD protection diodes are connected in series, across the shunt capacitor. The diodes are always reverse biased under normal operating condition of the circuit. If the transient voltage is outside of the range (-1V, + 6V), the diode clamps. The clamping establishes an alternate path to ground for the transient overvoltage, thus protecting the capacitor. The device is protected from ESD contact discharges up to 30KV per IEC61000-4-2 for the output pins of the PACSZ1284.

This device is connected directly to the parallel port and has very high probability of experiencing ESD events by the end- user, therefore this protection is essential.

Conclusion

California Micro Devices offers a family of products compliant with the IEEE 1284 recommendation that save board space and ease the manufacturing. The PACSZ1284 provides an integrated solution and guarantee the greatest ESD protection up to 30KV on the IEC61000-4-2 standard, combined with termination and filtering needed in your application.

References

[1] PACSZ1284 datasheet, California Micro Devices.

[2] PACS1284 datasheet, California Micro Devices.

[3] PACSE1284 datasheet, California Micro Devices.

[4] IEEE Standard 1284, December 1994.

[5] Motorola Semiconductor Application Note, Doc. AN1051/D, 1990.

[6] Ott, Henry, “Noise reduction techniques in electronic systems”, 2nd ed., Wiley Interscience, 1998, ISBN 0-471-85068-3.

[7] Pace, Charles, “Terminate bus lines to avoid overshoot and ringing”, *EDN*, vol.32, no.19, pp.227-34, Sept. 17, 1987.

[8] Royle, Dave, “Designer’s guide to transmission lines and interconnections”, *EDN*, vol.33, no.13, pp.131-160, June 23, 1988.