



512K x 32 CMOS High Speed Static RAM

FEATURES

- DSP Memory Solution
 - Motorola DSP96002
 - Analog SHARC DSP
 - Texas Instruments TMS320C3x, TMS320C4x
- Random Access Memory Array
 - Fast Access Times: 12*, 15, 17, and 20ns
 - TTL Compatible Inputs and Outputs
 - Fully Static, No Clocks
- Surface Mount Package
 - 68 Lead PLCC, No. 99 JEDEC M0-47AE
 - Small Footprint, 0.990 Sq. In.
 - Multiple Ground Pins for Maximum Noise Immunity
- Single +5V (±5%) Supply Operation

* Advance Information.

DESCRIPTION

The EDI8L32512C is a high speed, 5V, 16 megabit SRAM. The device is available with access times of 12, 15, 17 and 20ns allowing the creation of a no wait state DSP memory solution. The high speed, 5V supply voltage and control lines make the device ideal for creating floating point DSP memory solutions.

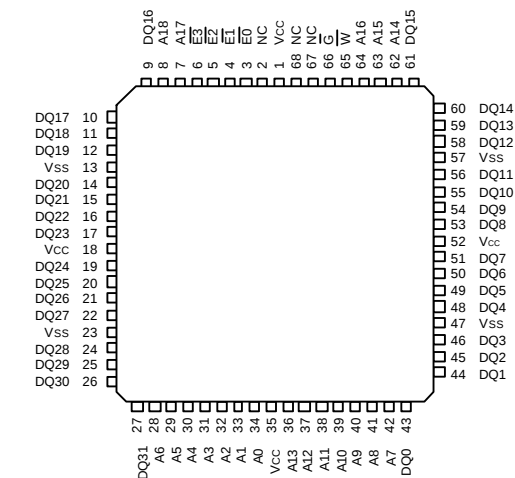
The device can be configured as a 512K x 32 and used to create a single chip external data memory solution for TI's TMS320C30/ C31 (Figure 8), TMS320C32 (Figure 9) or TMS320C4x (Figure 10), Motorola's DSP96002 and Analog's SHARC DSP (Figure 11). Alternatively, the device's chip enables can be used to configure it as a 1M x 16. A 1M x 48 program memory array for Analog's SHARC DSP is created using three devices (Figure 12). If this memory is too deep, two 512K x 24s (EDI8L24512C) can be used to create a 512K x 48 array or two 128K x 24s (EDI8L24128C) can be used to create a 128K x 48 array.

The device provides a 56% space savings when compared to four 512K x 8, 36 pin SOJs. In addition the EDI8L32512C has only a 10pF load on the data lines vs. 32pF for four plastic SOJs.

The device provides a memory upgrade of the EDI8L32256C (256K x 32) or the EDI8L32128C (128K x 32). For additional upgrade information see Figure 13.

Note: Solder Reflow Temperature should not exceed 230°C for 10 seconds.

FIG. 1 PIN CONFIGURATIONS AND BLOCK DIAGRAM



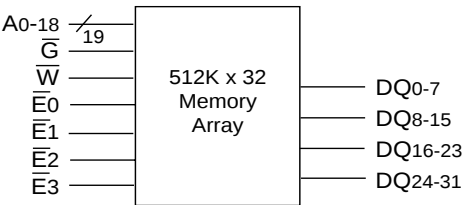
Note: For memory upgrade information, refer to Page 8, Figure 13 "EDI MCM-L Upgrade Path."

PIN NAMES

A0-18	Address Inputs
$\overline{E}0-3$	Chip Enables (One per Byte)
$\overline{W}$	Master Write Enable
$\overline{G}$	Master Output Enable
DQ0-31	Common Data Input/Output
Vcc	Power (+5V ±5%)
Vss	Ground
NC	No Connection

BYTE CONTROL TABLE

Chip Enable	Byte Control
$\overline{E}0$	DQ0-7
$\overline{E}1$	DQ8-15
$\overline{E}2$	DQ16-23
$\overline{E}3$	DQ24-31





ABSOLUTE MAXIMUM RATINGS*

Voltage on any pin relative to Vss	-0.5V to 7.0V
Operating Temperature TA (Ambient)	
Commercial	0°C to +70°C
Industrial	-40°C to +85°C
Storage Temperature	-55°C to +125°C
Power Dissipation	5.0 Watts
Output Current	20 mA
Junction Temperature, TJ	175°C

*Stress greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions greater than those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

Parameter	Sym	Min	Typ	Max	Units
Supply Voltage	Vcc	4.75	5.0	5.25	V
Supply Voltage	Vss	0	0	0	V
Input High Voltage	VIH	2.2	–	Vcc+0.5	V
Input Low Voltage	VIL	-0.3	--	0.8	V

AC TEST CONDITIONS

Input Pulse Levels	Vss to 3.0V
Input Rise and Fall Times	5ns
Input and Output Timing Levels	1.5V
Output Load	Figure 2

(Note: For TEHQZ, TGHQZ and TWLQZ, CL = 5pF)

FIG. 2

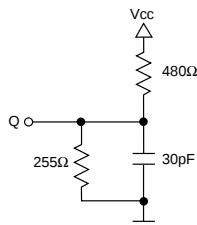
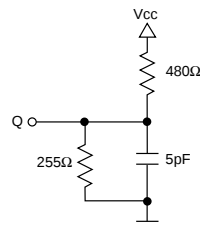


FIG. 3



DC ELECTRICAL CHARACTERISTICS

Parameter	Sym	Conditions	Min	Max		Units
				12/15	17/20	
Operating Power Supply Current	Icc1	$\overline{W} = V_{IL}$, I/O = 0mA, Min Cycle		800	720	mA
Standby (TTL) Supply Current	Icc2	$E \geq V_{IH}$, $V_{IN} \leq V_{IL}$ or $V_{IN} \geq V_{IH}$, $f = 0$ MHz		200	200	mA
Full Standby CMOS Supply Current	Icc3	$\overline{E} \geq V_{cc} - 0.2V$ $V_{IN} \geq V_{cc} - 0.2V$ or $V_{IN} \leq 0.2V$		40	40	mA
Input Leakage Current	II	$V_{IN} = 0V$ to V_{CC}		±10		μA
Output Leakage Current	ILO	$V_{IO} = 0V$ to V_{CC}		±10		μA
Output High Voltage	VOH	IOH = -4.0mA	2.4			V
Output Low Voltage	VOL	IOL = 8.0mA		0.4		V

TRUTH TABLE

$\overline{G}$	$\overline{E}$	$\overline{W}$	Mode	Output	Power
X	H	X	Standby	High Z	Icc2 Icc3
H	L	H	Output Deselect	High Z	Icc1
L	L	H	Read	DO _{UT}	Icc1
X	L	L	Write	DI _N	Icc1

CAPACITANCE (f=1.0MHz, VIN=Vcc OR Vss)

Parameter	Sym	Max	Unit
Address Lines	CI	30	pF
Data Lines	CD/Q	10	pF
Write & Output Enable Lines	$\overline{W}$, $\overline{G}$	30	pF
Chip Enable Lines	$\overline{E}$ -3	8	pF



AC CHARACTERISTICS READ CYCLE

Parameter	Symbol		12ns*		15ns		17ns		20ns		Units
	JEDEC	Alt.	Min	Max	Min	Max	Min	Max	Min	Max	
Read Cycle Time	TAVAV	TRC	12		15		17		20		ns
Address Access Time	TAVQV	TAA		12		15		17		20	ns
Chip Enable Access Time	TELQV	TACS		12		15		17		20	ns
Chip Enable to Output in Low Z (1)	TELQX	TCLZ	3		3		3		3		ns
Chip Disable to Output in High Z (1)	TEHQZ	TCHZ		6		7		9		9	ns
Output Hold from Address Change	TAVQX	TOH	3		3		3		3		ns
Output Enable to Output Valid	TGLQV	TOE		6		7		9		9	ns
Output Enable to Output in Low Z (1)	TGLQX	TOLZ	0		0		0		0		ns
Output Disable to Output in High Z(1)	TGHQZ	TOHZ		6		7		9		9	ns

*Advanced Information

Note 1: Parameter guaranteed, but not tested.

FIG. 4 READ CYCLE 1 - $\overline{W}$ HIGH, $\overline{G}$, $\overline{E}$ LOW

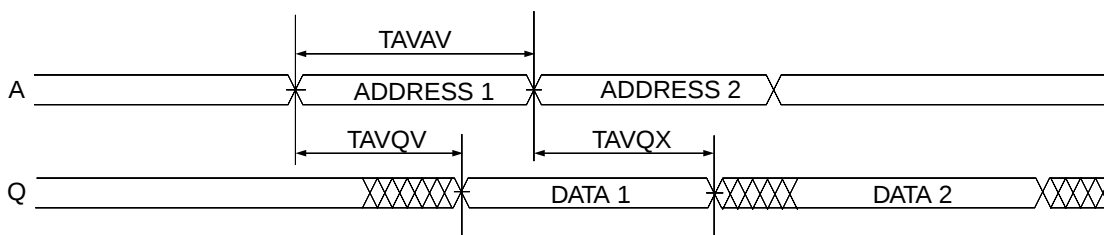
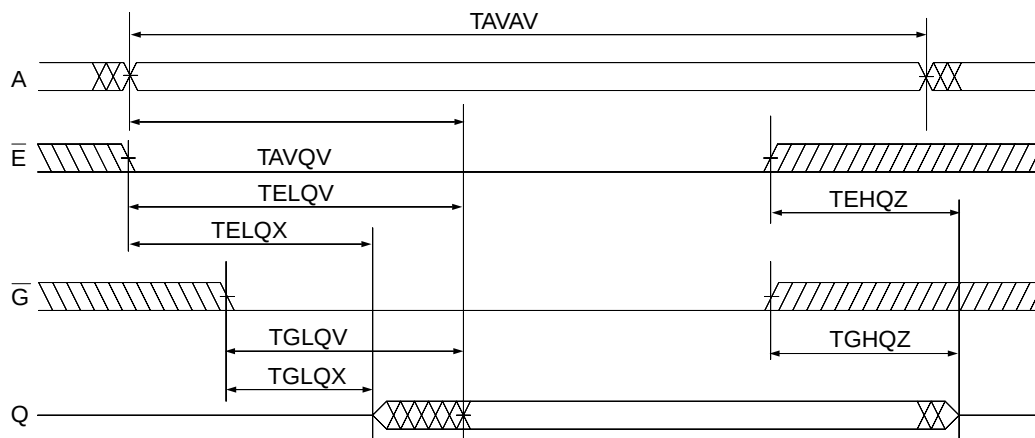


FIG. 5 READ CYCLE 2 - $\overline{W}$ HIGH





AC CHARACTERISTICS WRITE CYCLE

Parameter	Symbol		12ns*		15ns		17ns		20ns		Units
	JEDEC	Alt.	Min	Max	Min	Max	Min	Max	Min	Max	
Write Cycle Time	TAVAV	TWC	12		15		17		20		ns
Chip Enable to End of Write	TELWH	TCW	8		10		11		12		ns
	TELEH	TCW	8		10		11		12		ns
Address Setup Time	TAVWL	TAS	0		0		0		0		ns
	TAVEL	TAS	0		0		0		0		ns
Address Valid to End of Write	TAVWH	TAW	8		10		11		12		ns
	TAVEH	TAW	8		10		11		12		ns
Write Pulse Width	TWLWH	TWP	8		10		11		12		ns
	TWLEH	TWP	10		12		13		14		ns
Write Recovery Time	TWHAX	TWR	0		0		0		0		ns
	TEHAX	TWR	0		0		0		0		ns
Data Hold Time	TWHDX	TDH	0		0		0		0		ns
	TEHDX	TDH	0		0		0		0		ns
Write to Output in High Z (1)	TWLQZ	TWHZ	0	6	0	7	0	8	0	9	ns
Data to Write Time	TDVWH	TDW	6		7		8		9		ns
	TDVEH	TDW	6		7		8		9		ns
Output Active from End of Write (1)	TWHQX	TWLZ	3		3		3		3		ns

*Advanced Information.

Note 1: Parameter guaranteed, but not tested.

FIG. 6 WRITE CYCLE 1 - $\overline{W}$ CONTROLLED

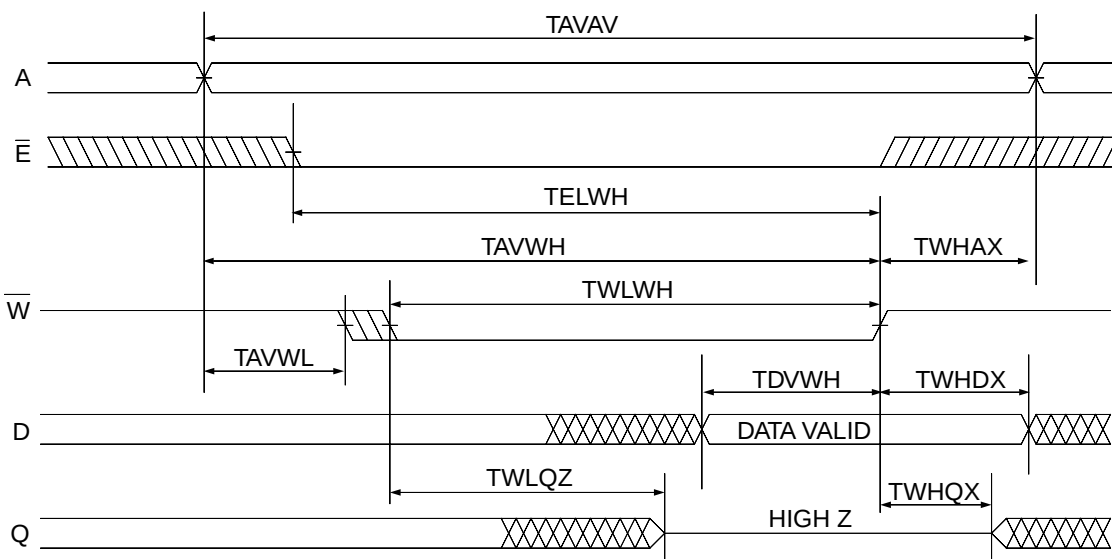
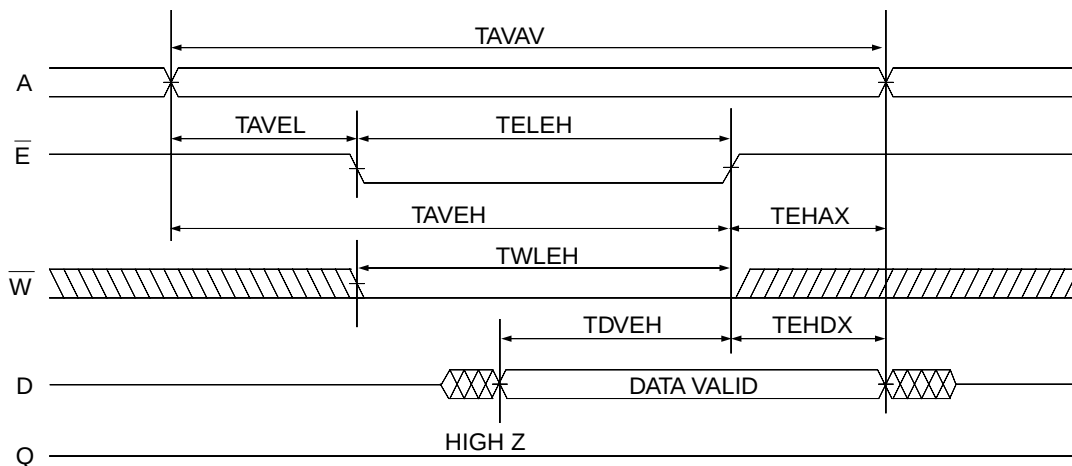




FIG. 7 WRITE CYCLE 2 - $\bar{E}$ CONTROLLED



ORDERING INFORMATION

Commercial (0°C to +70°C)

Part Number	Speed (ns)	Package No.
EDI8L32512C12AC*	12	99
EDI8L32512C15AC	15	99
EDI8L32512C17AC	17	99
EDI8L32512C20AC	20	99

Industrial (-40°C to +85°C)

Part Number	Speed (ns)	Package No.
EDI8L32512C15AI*	15	99
EDI8L32512C17AI	17	99
EDI8L32512C20AI	20	99

* Advance Information

PACKAGE DRAWING

Package No. 99

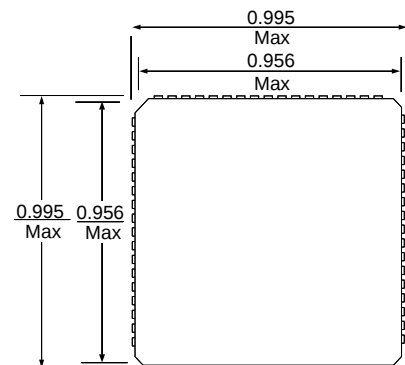
68 Lead PLCC

JEDEC MO-47AE

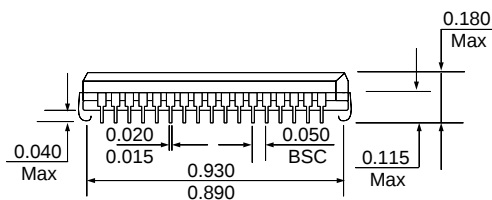
Weight = 4.2g

Theta JA = 40°C/W

Theta Jc = 15°C/W



Package No. 99
68 lead PLCC



Coplanarity (lowest lead to highest lead) 0.004



FIG. 8 INTERFACING THE TEXAS INSTRUMENTS TMS320C30/31 WITH THE EDI8L32128C (128KX32) OR THE EDI8L32512C (512KX32)

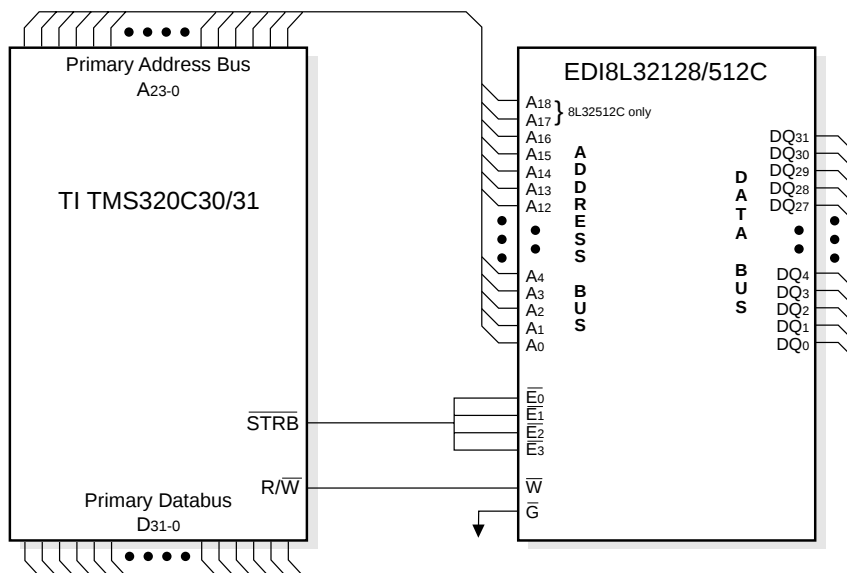


FIG. 9 INTERFACING THE TEXAS INSTRUMENTS TMS320C32 WITH THE EDI8L32128C (128KX32) OR THE EDI8L32512C (512KX32)

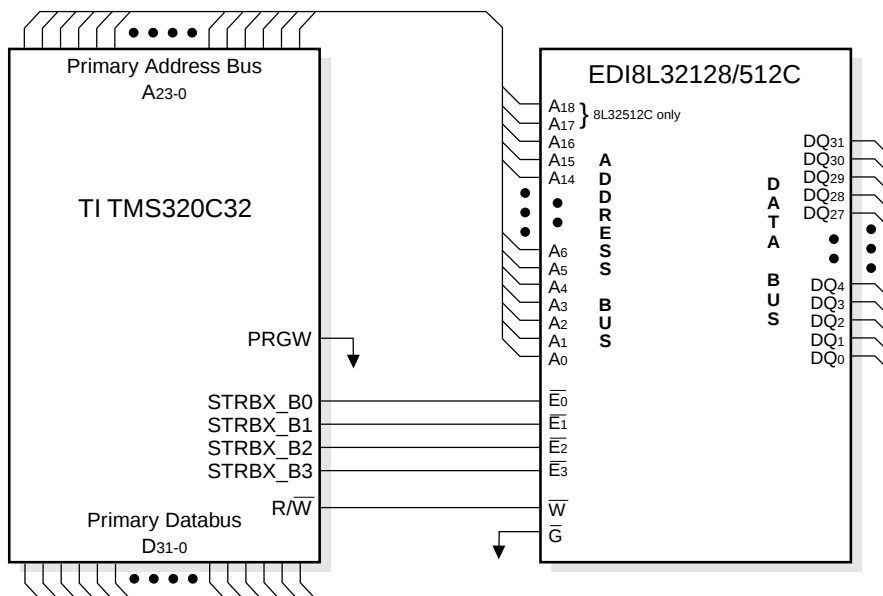




FIG. 10 INTERFACING THE TEXAS INSTRUMENTS TMS320C4x WITH THE EDI8L32128C (128KX32) OR THE EDI8L32512C (512KX32)

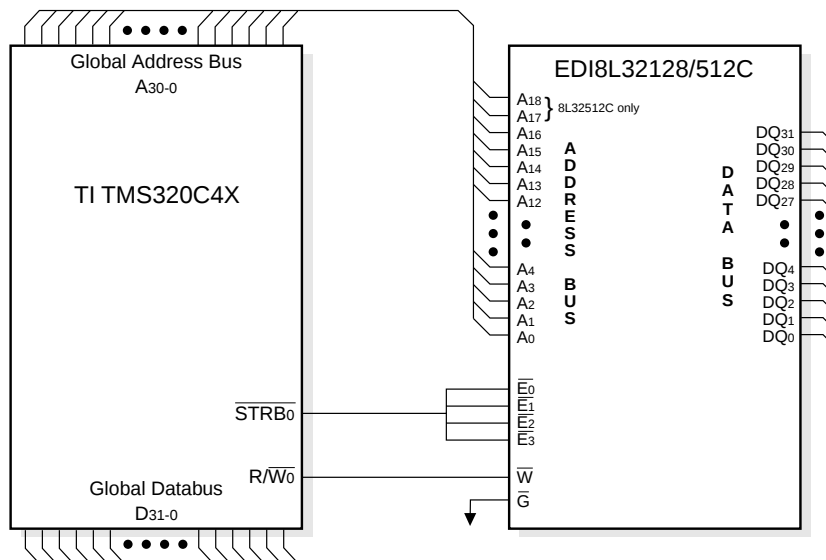


FIG. 11 INTERFACING THE ANALOG SHARC DSP WITH THE EDI8L32512C (512KX32)

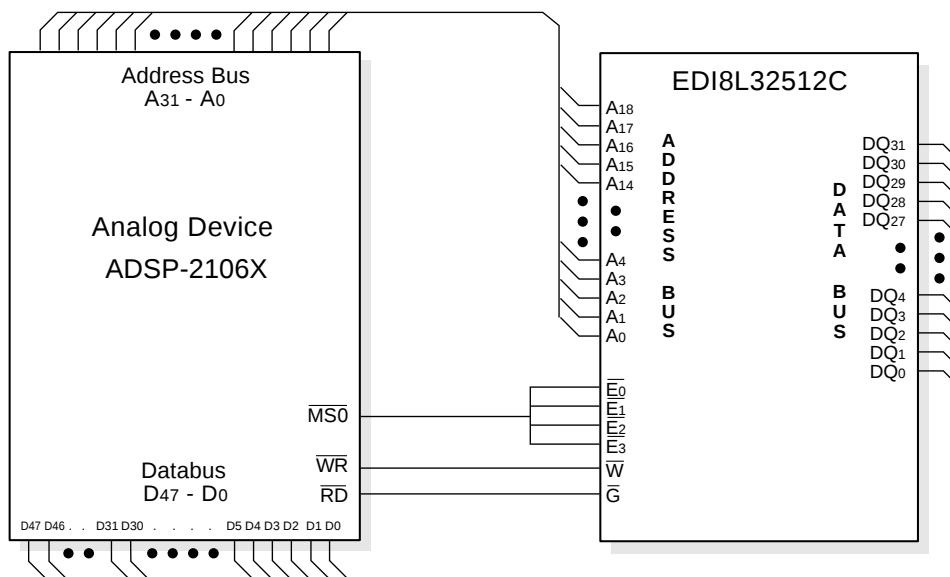




FIG. 12 INTERFACING THE ANALOG SHARC DSP WITH THE EDI8L32512C (1MX48)

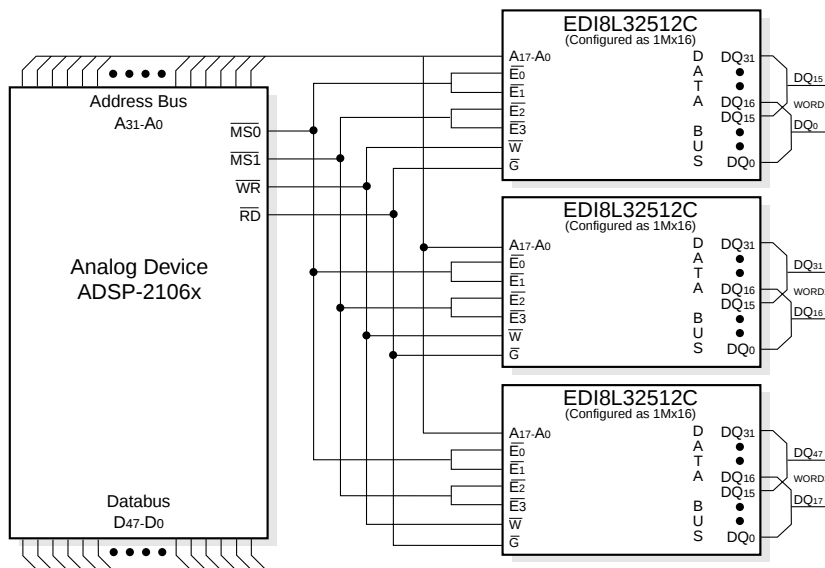


FIG. 13 EDI MCM-L UPGRADE PATH

